



PHD

Fabrication and Characterization of GaN grown on Silicon Vertical Structure Light Emitting Diodes

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Award date:
2017

Awarding institution:
University of Bath

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Fabrication and Characterization of GaN grown on Silicon Vertical Structure Light Emitting Diodes

submitted by

Paulo Ki

Dissertation presented in partial fulfilment of the requirements for the
degree of Doctor of philosophy

University of Bath

Department of Electrical and Electronic Engineering

Dec 2016

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Signature of Author..... Paulo Ki.....

**To my mother Vai Chi Mak, wife Kelly
Ki and Ao b Ao bb**

這論文是獻給你們的

Acknowledgement

Doing a PhD at the University of Bath was the most enjoyable time of my life besides the time I was at school in Macau. I would like to take this opportunity to express my acknowledge to the people who have contributed this experience to me. This work would not have been possible without their contribution.

First, I would like to express my deepest sincerely appreciation to my supervisor Dr. Duncan Allsopp for offering me an opportunity to do my PhD research and his advise for the research direction, issues during LED device fabrication and suggestions to improve the thesis.

Also, I would like to deeply thank Dr. Sivapathasundaram Sivaraya and Dr. Quanzhong Jiang for their patience for listening to me, help in the LED fabrication process and offering valuable advise on the research work. They are not only my work colleagues, but also my one of my best friends.

Finally and mostly importantly, I would like to thank my parents and my wife for their continuous encouragement and patience to listen when I was feeling depressed and wanted to give up. This work would have been much more challenging without them.

Thank you very much all again.

Paulo Ki

Abstract

III-Nitride semiconductor materials have been widely used for light emitting diodes (LEDs) for a wide range of lighting applications due to their excellent chemical stability and direct wide band gap energy nature. InGaN/GaN LEDs are conventionally grown on sapphire substrates with lateral contact device structure. However, LEDs fabricated with lateral contact device structure suffer from current crowding issue at the mesa boundary and contact edge when current flowing from the p-type GaN to n-type GaN, resulting in localized heating which reduces the internal quantum efficiency. In addition, sapphire substrates are relatively expensive and have a low thermal conductivity of 35 W/mK. Therefore, domestic LED lighting manufacturers have recently changed their interests to growing InGaN/GaN LEDs on Silicon (Si) substrates rather than sapphire substrates. Si substrates not only have higher thermal conductivity (i.e. 149 W/mK), but are also cheaper than sapphire substrates. However, Si substrates are light absorbing; if LEDs fabricated with conventional lateral contact structure the emitted light, which travels toward the Si growth substrate, is absorbed and wasted. To resolve this issue, the vertical LED (VLED) structure is adopted for InGaN/GaN LED grown on Si substrates. The original Si growth substrate is removed and the InGaN/GaN LED epitaxy is bonded on to a Si carrier substrate with a reflectivity p-type ohmic contact.

In this thesis, a complete fabrication process of InGaN/GaN grown on Si VLEDs with a novel reflective p-contact was developed and characterized. A reflective p-type ohmic contact of Ni/Ag/Ni was developed to act as a mirror, which prevents the light absorption by the Si carrier substrate. This contact has a high reflectivity of 75% and a low contact resistivity of $6.3 \times 10^{-5} \Omega \text{cm}^2$ after annealing in an oxygen environment for 2 minutes at 450 °C to form an ohmic contact to p-GaN. The light output power of our VLED using Ni/Ag/Ni contact is approximately 20 mW higher than the VLEDs without any reflectors fabricated by Xiong et. al.. Although the forward voltage of our VLEDs is 0.5 V higher than VLEDs made by Xiong et. al., this can be attributed to our Si carrier substrates do not have any thickness reduction process. The impact of the thickness of Si

carrier substrate on the electrical and optical performance of the VLED was also characterized. By using a Si carrier substrate with a thickness of 475 μm rather than 675 μm , the quantum confined stark effect was reduced and the external quantum efficiency was improved by 4 %. Also, the operational voltage was reduced to 5.7 V from 6.7 V at the drive current of 300 mA. Finally, a KOH surface roughen process for the N face n-GaN was devised to resolve the total internal reflection issue at the interface between the n-GaN and air. The light output power of the VLED increased from 53 mW to 97 mW after etching in 4M KOH solution at 100 °C for 3 minutes.

List of Abbreviations

| | |
|------------------|--|
| Ag | Silver |
| Al | Aluminum |
| AlGaN | Aluminum Gallium Nitride |
| Au | Gold |
| Be | Beryllium |
| Cd | Cadium |
| CTLM | Circular Transmission Line Model |
| DPL | Dynamic Photoluminescence |
| EBE | Electron Beam Evaporation |
| EQE | External Quantum Efficiency |
| Ga | Gallium |
| GaN | Gallium Nitride |
| GLE | GaN-based LED Epitaxy |
| HCl | Hydrochloride Acid |
| HF | Hydrofluoric Acid |
| HNO ₃ | Nitric Acid |
| HVPE | Hydride Vapour Phase Epitaxy |
| ICP | Inductive Coupled Plasma |
| In | Indium |
| InGaN | Indium Gallium Nitride |
| KOH | Potassium Hydroxide |
| LED | Light Emitting Diodes |
| LEE | Light Extraction Efficiency |
| Mg | Magnesium |
| MOCVD | Metal Organic Chemical vapor Deposition |

| | |
|------------------|---|
| MQW | Multiple Quantum Well |
| N | Nitrogen |
| Ni | Nickel |
| NiO | Nickel Oxide |
| PECVD | Plasma Enhanced Chemical Vapour Deposition |
| Pt | Platinum |
| RMS | Root Mean Square |
| SEM | Scanning Electron Microscope |
| Si | Silicon |
| SiC | Silicon Carbide |
| SiO ₂ | Silicon Dioxide |
| Sn | Tin |
| Ti | Titanium |
| VLED | Vertical Light Emitting Diode |
| WPE | Wall-plug Efficiency |

List of Symbols

| | |
|----------------------|--|
| A | Contact area |
| A^* | Richardson's constant |
| d | Distance between inner and outer test contact pad |
| E_F | Fermi energy |
| E_g | Bandgap energy of semiconductor |
| ρ_c | Specific Contact Resistivity |
| ϕ_{p-GaN} | Workfunction of p-GaN |
| ϕ_m | Workfunction of metal |
| ϕ_s | Workfunction of semiconductor |
| ϕ_B | Schottky barrier height |
| E_g | Bandgap energy of semiconductor |
| ϵ_s | dielectric constant of the semiconductor |
| χ | Electron affinity of semiconductor |
| h | plank's constant |
| i | Current flow across separation d |
| J | Current density |
| m_H | mass of holes |
| m_E | mass of electrons |
| N_A | Doping concentration of acceptors |
| R_c | Contact resistance |
| R_s | Sheet resistance of semiconductor |
| T | Temperature in Kelvin |
| L_T | Transfer length |
| I_0, I_1, K_0, K_1 | Modified bessel function |
| r_i, r_o | Inner and outer radii of CTLM |
| W | Width of depletion region |

| | |
|------------|--|
| q | Charge of electrons |
| S_T | Thermal stress |
| ν | poisson rate |
| α_f | Thermal expansion coefficient of the film |
| α_G | Thermal expansion coefficient of GaN |
| ΔT | Change of temperature in Kelvin |
| π | The ratio of a circle's circumference to its diameter |

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Chapter 1

Introduction

The rise in energy demand is one of the major concerns of mankind besides the shortages of food and water due to the rapid growth in world population. The growth of global energy demand is forecast to exceed the energy production in the near future [1]. Globally about 20 percent of electricity consumption is accounted for traditional lighting systems. As a result, a significant amount of energy can be saved if inefficient lighting technology can be replaced with a more efficient lighting system. A Light Emitting Diode (LED), which is expected to be the most efficient light source and is the best candidate to replace all the traditional light sources [2], is made using semiconductor materials that have many similar properties to the chips on computer motherboards. The only major difference is that the semiconductor used in LEDs emit light. Conventional light source generally refers to incandescent and fluorescent light bulbs. Traditional light bulbs emit light by incandescence, which is a visible electromagnetic radiation emitted by heating a tungsten filament to a high temperature, usually above 750°C [2]. Whereas, the fluorescent light bulbs emit white light by exciting mercury gas using electricity to produce UV light, the phosphor coating on the glass tube then absorbs the UV light and re-emits white light [3]. Although fluorescent light bulbs (67 lm/w) are nearly as efficient as LEDs (85 lm/w) [2], the disposal of the mercury used within its manufacturing process creates an environmental hazard. A considerable amount of energy is wasted to produce heat during the light generation process in incandescent light sources and, as mentioned, the mercury in fluorescent light sources is environmental hazard. However, the structure of an LED and the way it generates light are fundamentally different from traditional light sources. It is a junction of p-type and n-type semiconductors that emits light through electron-hole radiative recombination. This light generation process can occur at room temperature and does not produce heat. The only contributions to generate heat in LEDs are

non-radiative recombination due to defects, surface states and Joule heating in any parasitic resistances, which means a much smaller amount of energy is wasted as heat. In addition, LEDs do not require a glass tube or gases to generate light. As a result, it is generally only composed of several layers of semiconductor materials and allows LEDs to have a smaller physical size compared to traditional light sources, which makes LEDs suitable for flat panel displays or electronic equipment requiring compact light sources, as well as novel lighting applications, for example, telescopic surgery in healthcare. LEDs can also typically last for 50,000 hours, which is 25 times the average lifetime of an incandescent light bulb and 5-10 times that of fluorescent light sources [3]. Thus, LEDs are very promising replacements for the traditional light sources.

Gallium Nitride (GaN), Aluminium Nitride (AlN) and Indium Nitride (InN), which together are known as III-Nitride compound semiconductors, have recently drawn a lot of researcher interest. They are known to have very good thermal, electrical and chemical stabilities, LEDs made using them can operate in harsh and high power conditions [3]. In, addition, they are direct band gap materials with respective room temperature band gap energies of ~3.4 eV (which is a near-UV photon), ~6.2 eV (a deep-UV photon) and ~0.7 eV (an infrared photon) respectively [4]. The wavelength emission of GaN LED can be changed continuously from near-UV (~3.4 eV) to blue (~2.64 eV) or green (~2.36 eV) by alloying GaN with InN to create $\text{In}_x\text{Ga}_{1-x}\text{N}_x$, where x is the mole fraction of InN in the alloy. Blue and green LEDs can therefore be created by alloying GaN with InN. The higher the In content in the InGaN alloy, the lower the energy of a photon is emitted. Whereas, the UV LEDs can be realized by alloying GaN with AlN as AlN has a higher band gap energy than GaN. Therefore, the entire spectrum from the deep UV to red can theoretically be covered by changing the composition of InGaN and AlGaN alloys. It is worth noting that GaN based materials have a continuous direct band gap across its entire alloy system given by

$$E_{ab}|_{\text{alloy}} = E_a + x(E_b - E_a) + x(1-x)E_b \quad (1.1)$$

Where E_a is the band gap energy of GaN, E_b is the band gap energy of InN or AlN and x is the mole fraction of the compound [3].

This means that LEDs made using GaN based materials can in principle achieve a high internal quantum efficiency, which is a ratio of radiative electron-hole recombination events to the total electron-hole recombination events. Thus, III-Nitrides are considered as the best semiconductor materials to be used for LED applications.

1.1.Motivation

Since the GaN native growth substrate is expensive, GaN based LED epitaxy is generally grown on sapphire substrates, which are electrically and thermally insulating. Since sapphire substrates are not electrically conducting, a lateral contact LED structure is generally used as shown in Figure 1.1(b). As a consequence, the current must travel laterally from n-type contact to the p-GaN layer in such structure from the contact, resulting in current crowding near the mesa edge under a high current density condition. This causes the LED to heat up locally, which reduces both the radiative recombination efficiency and the effective emissive area. Despite Silicon (Si) substrates have a large lattice constant mismatch of 17 % and thermal expansion coefficient of 55 % to GaN [5], researchers and manufacturers are moving their research interests from growing GaN based LEDs on sapphire to Si substrates of (111) orientation in recent years as it is electrically conducting and available at large size with a much lower cost [6]. Growing GaN based LEDs on Si substrates with (111) orientation is preferred as the Si substrates in this orientation have a hexagonal symmetry and wurtzite GaN can be obtained. It is worth knowing that Si substrates (149 W/mK) are not only cheaper, but also more thermally conducting than sapphire substrates (35 W/mK), which allows better heat dissipation, leading to a higher radiative recombination rate [3]. The high electrical conductivity of Si substrate allows an electrical connection to be put on the backside of the Si wafer, so a vertical LED (VLED) structure can be realized as illustrated in Figure 1.1(a). The VLED structure has many advantages, for instance, lower series resistance, better heat dissipation and higher, more uniform injection current density. In particular, it can eliminate the

mesa edge current crowding problem as current now flows vertically rather than laterally.

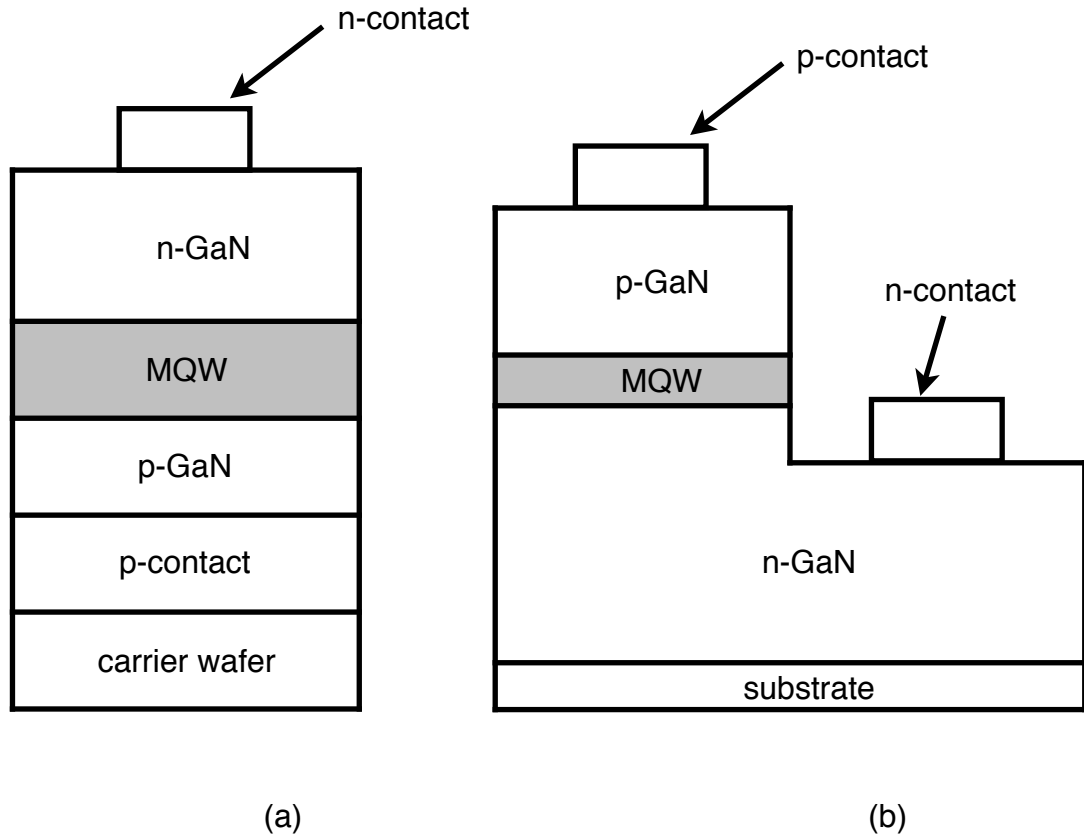


Figure 1.1: Generic structures of (a) a vertical and (b) lateral contact LEDs.

However, the Si substrate is not transparent in the visible light spectrum, so emitted light that propagates to the substrate, is most likely absorbed, leading to the reduction in the light extraction efficiency (LEE). As a result, the original growth Si substrate is removed during the LED fabrication process and the LED epitaxy is then bonded on to a Si carrier substrate with a reflective metal contact (usually p-type contact) in between the LED epitaxy and the Si carrier substrate. It is worth knowing that Si with (100) orientation is preferred for carrier substrate as it can be sawn and cleaved into square shape. Whereas Si with (111) orientation tends to cleave into triangles. The p-type contact is then required to be reflective (Note: GaN on Si vertical LEDs are p-side down and n-side up), so the light emitted by the active region is reflected by the p-type contact rather than being absorbed by the substrate.

The purpose of this work was to fabricate and characterize an InGaN/GaN LEDs grown on Si with vertical structure. The first objective was to develop a thermally stable and highly reflective p-type ohmic contact, which is able to remain low resistant and highly reflective after high temperature wafer bonding process to a carrier substrate. This is very important as the trend to higher temperature wafer bonding processes, to improve LED packaging reliability, gives rise to concerns about the integrity and the stability of reflecting contacts on p-type GaN. The secondly main objective was to examine the impact of Si carrier substrate thickness on the electrical and optical device performance. Finally, although VLED has a larger emissive area than conventional lateral contact LEDs, having a good light extraction efficiency is still required in VLEDs. This is because the light still escapes from the top surface of GaN material, it is still suffered from the small critical angle of $\sim 23^\circ$ between the boundary of GaN and air and the n-contact partially blocking light emission through the top surface of the device. This led to the final objectives of characterizing the light output and n-type contact resistivity on Potassium hydroxide (KOH) roughened N face n-GaN surfaces used to enhance light extraction. It is believed that meeting these objectives represents innovation in GaN based LED fabrication.

1.2. Outline of thesis

This thesis discusses the fabrication process and characterization of InGaN/GaN grown on Si vertical LED. The thesis content is structured as follows:

Chapter 1 has provided a brief introduction to InGaN/GaN LED and to the motivation of the work.

Chapter 2 discusses the foundation physics of LEDs and the GaN material.

Chapter 3 discusses the device fabrication process and experimental techniques used in this work.

Chapter 4 discusses the investigation of p-type reflective ohmic particularly for the application of VLED. The electrical and optical properties of Ag based contacts were studied at the temperature range of 300 °C to 500 °C in the step

of 50 °C, so as to optimise the Ag contact metallisation scheme. Current-voltage (I-V), light output power to current (L-I), and surface topologies of the contacts are analyzed.

Chapter 5 discuss the investigation of thermal stability of Ni/Au/Ag based contacts on VLEDs at 450 °C for 30 minutes in an air ambient to stimulate the worse case scenario of wafer bonding.

Chapter 6 reports the study of the impact of Si carrier substrate thickness on the electrical and optical properties of VLEDs after the LED epitaxy being transferred. The stress of the LED epitaxy before and after the transfer were studied by using dynamic photoluminescence technique, MQW PL and curvature of the VLED. The optical and electrical properties of the VLED were studied by using I-V and L-I measurements.

Chapter 7 investigates the effect of potassium hydroxides (KOH) surface roughening N face n-GaN of the VLED. The contact resistivity of Ti/Al/Ni/Au on KOH roughened n-GaN with various KOH concentration was studied. VLEDs with n-GaN surface roughened by 2M, 3M and 4M KOH solutions were fabricated, so as to study the actual impact of the surface topology.

Chapter 8 summarises the main findings of this work and gives a recommendation for future work.

1.3.References

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Chapter 2

III-Nitride Based LEDs

2.1. Evolution of LEDs

In 1907, the British scientist, Henry Joseph Round, became the first person to observe accidentally blue light emissions from Silicon Carbide (SiC) crystals caused by applied electric fields during an investigation of crystal detectors [1]. This was accidental, so the light emission mechanism was not understood and the quality of SiC film was not well controlled at that time.

In 1923, sixteen years after the first observation of electroluminescence from SiC crystals, the first LED was made during an investigation of the cause of light emission from SiC by the Russian scientist, Oleg Vladimirovich Losev [1]. By the late 1960s, device fabrication and preparation of SiC film techniques were more developed, which allowed the first practical blue LED to be made using SiC by Violin et al [2]. However, the wall-plug efficiency, which measures the efficiency of converting electrical power into optical power, was just 0.005 % [1]. The wall-plug efficiency of blue SiC LEDs has never had a significant improvement as SiC is an indirect band gap semiconductor material. Indeed the wall-plug efficiency of the best blue SiC LED achieved is only 0.03 % [3]. Therefore, until now blue LEDs made using SiC have never been practically used for lighting applications. Another material and process technology were needed.

III-V compound semiconductors were unknown substances before the 1950s as they do not exist naturally. They were first introduced by Heinrich Welker in 1952 [1]. Ten years later, in 1962, an infrared LED was made using Gallium Arsenide (GaAs) [1]. Since GaAs has a band gap energy equal to the energy of an infrared photon (1.42 eV), LEDs made using pure GaAs semiconductor do

not emit in the visible spectrum. To create LEDs emitting in visible spectrum, GaAs is alloyed with Aluminium or Phosphorus to form AlGaAs or GaAsP, which have a higher band gap energy than GaAs. So the colour of light emission can be changed from infrared to the yellow-red part of the visible spectrum by increasing the composition rate of Al in the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ alloy; the higher the Al content, the higher the photon energy is emitted. AlGaAs ternary material system was the main material used for high brightness red and infrared LEDs in the 1980s [1]. On the other hand GaP, whilst being an indirect band gap semiconductor, emits light in the green part of the spectrum (photon energy ≈ 2.140 eV) via the formation of an impurity level associated with Nitrogen (N) impurities [1].

Since AlGaAs LEDs only emit in the spectrum from infrared to yellow-red, it cannot be used for high brightness green LEDs or shorter wavelength emitters. Aluminium Gallium Indium Phosphide (AlGaInP) quaternary material system was then introduced in 1985. Theoretically, It can emit red, orange, yellow or green light when the composition rate is adjusted correctly. However, $(\text{Al}_x\text{Ga}_{1-x})_{0.5}\text{In}_{0.5}\text{P}$ cannot be used for green LEDs as its band gap becomes indirect when the Al composition rate exceeds 53 %. Therefore, it is not suitable for high brightness green LEDs and can only be used to fabricate high brightness red, orange and yellow LEDs. A red LED with luminous efficiency as high as 100 lm/W has been realized using AlGaInP material system [1]. Until 1990's this limited the application of LEDs to mainly displays and on-off indicators.

In general, white light is required for most space or general lighting applications. There are two ways to create white light. The first method is to use a blue LED with a phosphor coating and the second method is to combine three primary colour LEDs (i.e. red, blue and green LEDs). Both methods require blue LEDs, so high brightness green and blue LEDs are essential for creating white light. High brightness red, orange and yellow LEDs can be fabricated using the above-mentioned AlGaAs and AlGaInP. However, there was no suitable direct band gap material with high enough band gap energy for fabricating high brightness green and blue LEDs until the blue Gallium Nitride (GaN) based LED was invented by Nakamura et. al. in 1994 [4]. The GaN compound

semiconductor reignited the hope of using LEDs for general light applications and opened up a completely new field of research.

GaN, AlN and InN belong to the III-V compounds semiconductor category and sometimes more specifically known as III-Nitride compound semiconductors. They are considered to be the best semiconductor materials for LEDs as they have a good electrical and chemical stability [4]. So that the LEDs made using GaN based materials can operate in a harsh environments and under high power conditions. In addition, GaN, AlN and InN are all direct band gap materials with their room temperature band gap energies of 3.4 eV (which is a near-UV photon), 6.2 eV (a deep-UV photon) and 0.7 eV (an infrared photon) respectively [5]. The wavelength emission of GaN can be changed from near-UV (3.4 eV) to blue (2.64 eV) or green (2.36 eV) by alloying GaN with InN. To enable the manufacture of LEDs emitting these colours. Blue and green LEDs can therefore be created by alloying GaN with InN. The higher the In composition rate in the InGaN alloy, the lower the energy of a photon is emitted. Whereas, the UV LEDs can be realized by alloying GaN with AlN as AlN has a higher band gap energy than GaN. Therefore, the entire visible spectrum ranging from violet to red can theoretically be covered by changing the composition rates of InGaN and AlGaN alloys. In addition, GaN based materials have a continuous direct band gap across its entire alloy system, meaning that LEDs made using GaN based materials can achieve high internal quantum efficiency.

However, it is worth noting that an $\text{In}_x\text{Ga}_{1-x}\text{N}$ active region with a high In content (i.e. $x > 0.35$) is difficult to grow as In-rich quantum dots (clusters) are formed during the growth [1] and the lattice constant of In-rich InGaN has a significant mismatch with that of GaN, as illustrated in Figure 2.1. Therefore, GaN based LEDs with an In-rich InGaN active region such as red LEDs are not generally used for long wavelength emitters. As a result, InGaN is generally used for the fabrication of high brightness blue and green LEDs. Whereas, high brightness red LEDs are made using AlGaInP.

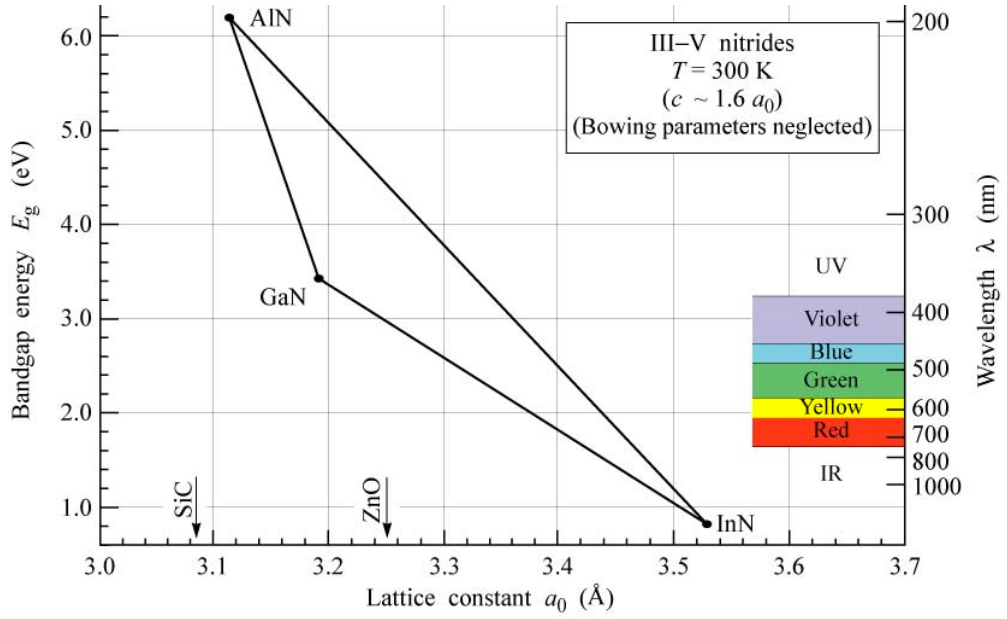


Figure 2.1: Band gap energies of III-Nitride semiconductors in wurtzite structure at room temperature [1].

2.2. General Properties of III-Nitride Semiconductors

It can be seen in Figure 2.1 that the change of band gap energies of III-Nitride compound semiconductors as a function of their lattice constants. This is a great advantage for LEDs as the tunable direct wide band gap feature enables the light emission of LEDs covering the entire visible spectrum ranging from violet to red to be realized using GaN based materials. Also, the direct band structure is essential for obtaining a high electron-hole radiative recombination rate, which is the light generation process in LEDs. In addition, the leakage current of III-Nitride compound semiconductors is low compared to mid-low band gap material as leakage current is proportional to the intrinsic carrier concentration, which is an exponential function of band gap energy and temperature as illustrated in equation (2.1) [1]

$$n_i = N_s \exp\left(\frac{-E_g}{2kT}\right) \quad (2.1)$$

In equation (2.1), N_s is the effective density of states, E_g is the band gap energy and k is Boltzman's constant. These materials also have a very high bond strength thanks to the large difference in electronegativity between group III atoms and N atoms. Owing to this high bond strength they do not degrade

easily at high temperature or under high current conditions. III-Nitride semiconductors are also excellent for operating in a harsh environment as they are chemically stable, and are not easily attacked by acids or alkalis [5]. Therefore, the III-Nitride compounds semiconductors have been considered as the best materials for high brightness green and blue LEDs.

2.3. Physical Properties of III-Nitrides Semiconductors

GaN, InN and AlN can crystalize in three different forms, which are the wurtzite, zinc-blende and rock salt crystal structures as shown in Figure 2.2. Although III-Nitride semiconductors naturally tend to crystallize in their most stable form, namely wurtzite crystal structure. The crystal structure of the substrate used during the epitaxial growth process also plays an important role in determining the crystal structure of III-Nitride semiconductors [6]. For instance, if a substrate with cubic symmetry such as Si [001] is used for GaN growth, the cubic structure of the substrate makes the GaN layers tend to crystallize in the zinc-blende structure. Whereas, if the GaN is grown epitaxially on sapphire [0001], which is a hexagonally symmetric facet substrate, it naturally tends to crystallize in the wurtzite crystal structure. The zinc-blende GaN has recently attracted researchers' attention as it has several advantages over the wurtzite GaN. For instance, the energy band gap of zinc-blende GaN (3.2 eV) is lower than that of wurtzite GaN (3.4 eV), so that a lower In content is required in the InGaN active region of GaN based LEDs. This is a huge advantage for the LEDs that require an In-rich active region such as green LEDs: a high In content InGaN active region is generally hard to grow due to the tendency of In to segregate during the growth and the increase of lattice constant of InGaN with In content, which causes the InGaN to become lattice mismatched with GaN and hence strained. In addition, as the crystal symmetry of zinc-blende GaN is better than that of wurtzite GaN: the electron and hole mobilities of zinc-blende GaN are higher than that of wurtzite GaN [5], which makes it attractive for transistor applications.

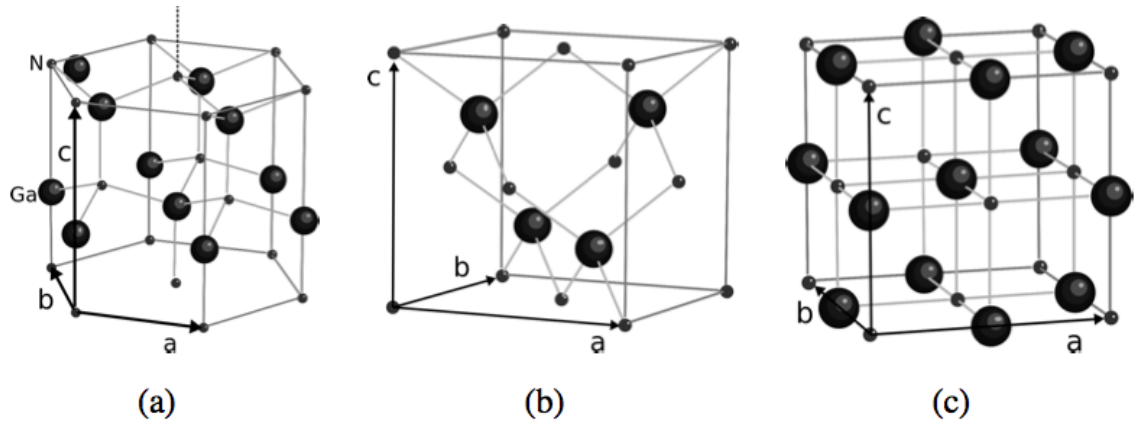


Figure 2.2: Crystal structures of GaN in (a) wurtzite, (b) zincblende and (c) rocksalt structures [7].

GaN, InN and AlN are different from the other common III-V semiconductors that are thermodynamically stable in the zinc-blende crystal structure at room temperature (e.g. GaAs). The III-Nitrides are most thermodynamically stable in the wurtzite structure and metastable in the zinc-blende structure at room temperature [8]. The wurtzite crystal structure is very similar to the zinc-blende crystal structure in terms of crystallography. The main difference between the two structures is the stacking sequence of the atomic planes. The stacking sequence of GaN in the wurtzite structure is ABABAB along the $[000\bar{1}]$ direction, while that in the zinc-blende structure is ABCABC along the $[111]$ direction, as illustrated in Figure 2.3. Since the wurtzite and zinc-blende crystal structures mainly only differ in stacking sequence, and due to stacking faults, zinc-blende GaN is often found in the GaN nucleation layer, which is generally grown at approximately 500 °C on a sapphire substrate [7]. In contrast to the wurtzite and zinc-blende structures, GaN in the rock salt structure only exists at pressure higher than 25 kbar [8].

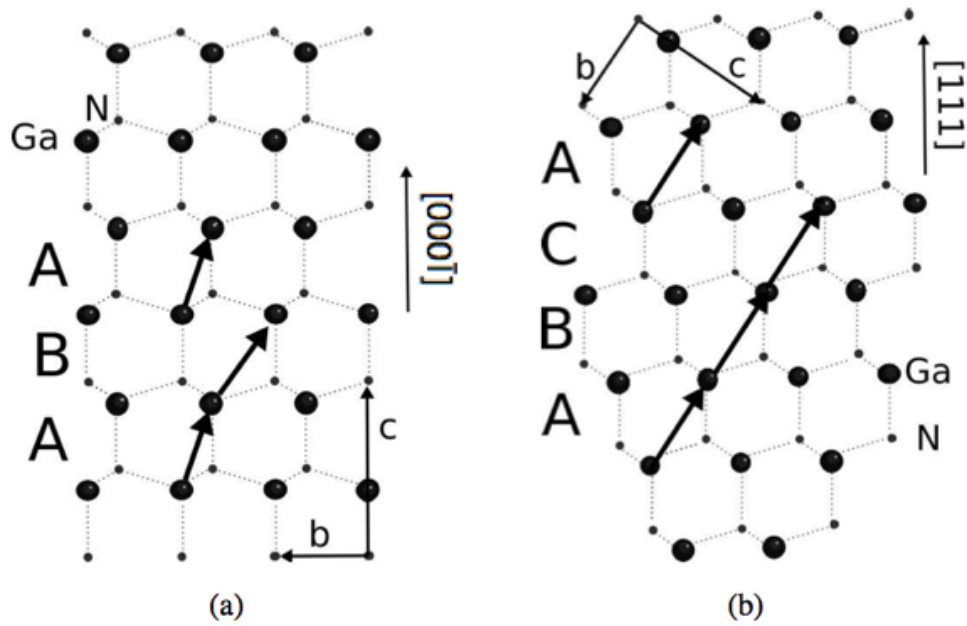


Figure 2.3: The stacking sequences of GaN in (a) wurtzite structure and (b) zincblende structure [7].

Although GaN substrate has recently been available, it is very expensive and time consuming to grow [6]. Consequently, there are no other suitable lattice match substrates, the growth of wurtzite GaN is most commonly performed on sapphire and SiC substrates, which are 13.9 % and 3.5 % lattice mismatched respectively [8]. Since sapphire substrates are less expensive, the growth of wurtzite GaN is normally performed on sapphire substrates along the c -axis (i.e. normal to the $[0001]$ basal plane). The top and bottom of the wurtzite GaN crystal are called basal planes with the edge length (a) of 3.189 Å and the sides of the crystal are called prism planes with the height (c) of 5.185 Å [8]. The atoms are structured in closely spaced hexagonal bilayers in this growth direction; one layer is made of Ga atoms (cations) and the other layer is made of N atoms (anions). Therefore, the bilayer in such structure has two different polarities and the surface of the basal plane can either be N-face (nitrogen face) or Ga-faced (gallium face). N face means that the atoms are nitrogen at the top position of the bilayer in $[000\bar{1}]$ direction and Ga-face means that the atoms are Ga at the top position of the bilayer in the $[0001]$ direction, as illustrated in Figure 2.4. It is worth noting that N-face does not mean that the bonds are terminated by N atoms as a Ga-face basal plane can also be terminated by N atoms if it is covered by nitrogen atoms.

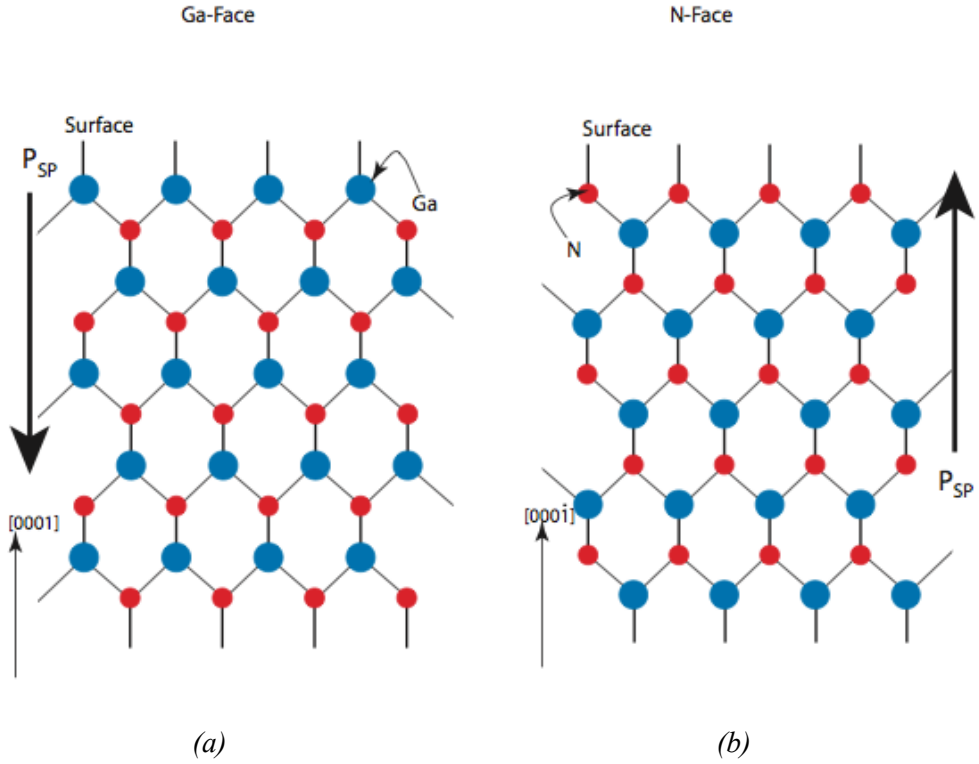


Figure 2.4: GaN in wurtzite crystal structure with (a) Ga-face and (b) N-face polarities [9].

The III-Nitride compound semiconductors are polar materials as they do not have inversion symmetry [8]. Therefore, they have polar axes, which means that the bonds along the polar axis are only faced by group III atoms (cations) in one direction and faced by only nitrogen atoms (anions) in the opposite direction. Since the polarity of the Ga atoms is different from that of the N atoms in the bilayer, this polarity difference sets up an internal electric field inside the GaN called the spontaneous polarization (SP) [8]. Furthermore, as GaN does not have centre of symmetry, it possesses piezoelectric polarization property, which is a strain induced polarization field [10]. The direction of the piezoelectric polarization depends on whether the GaN is under tensile or compressive strain. In the the quantum well active region within the LED, the electric field caused by these two polarizations can seriously influence the shape of the quantum well potential and induce a spatial separation of electrons and holes inside the quantum well. Thus, the rate of radiative recombination can be influenced by piezoelectric and spontaneous polarization, lowering the internal quantum efficiency.

In addition to the polarization mentioned above, the properties of GaN can also be influenced by the polarity of the basal plane. For instance, N-face GaN is

less chemical stable than Ga-face GaN, so the etch rate of N-face GaN is faster [7]. Also, it is more difficult to fabricate devices on N-face GaN than Ga-face GaN as the N-face GaN surface is a lot rougher than Ga-face GaN, as illustrated in Figure 2.5(b).

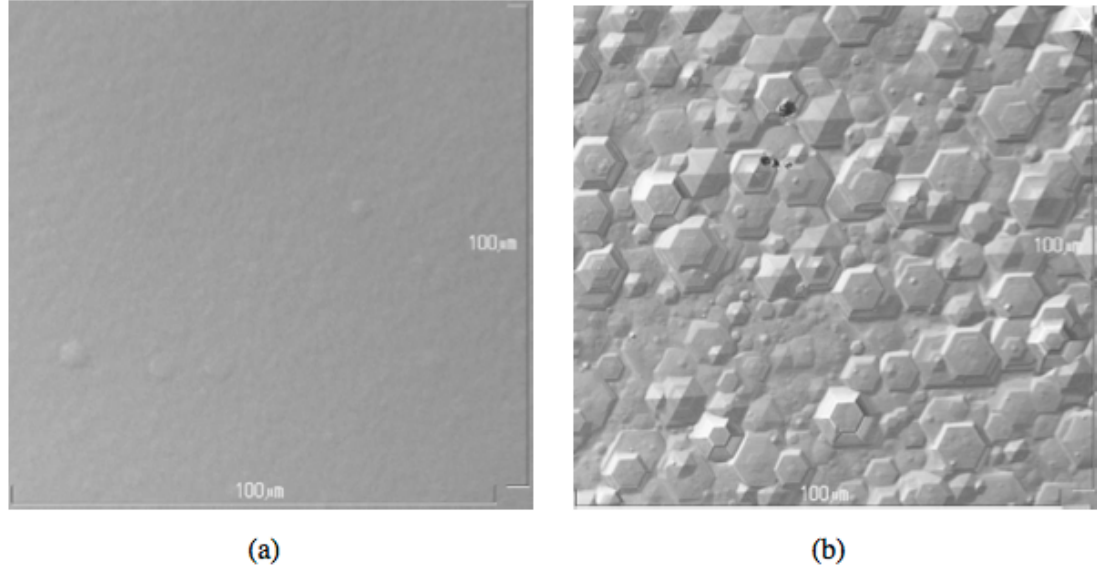


Figure 2.5: Optical microscope image ($100\ \mu\text{m} \times 100\ \mu\text{m}$) of (a) Ga-face GaN and (b) N-face GaN [7].

The properties of III-Nitride compound semiconductor properties are summarized in Table 2.1. It can be seen that the lattice constants between III-Nitride semiconductors vary significantly. For instance, if GaN is grown on unstrained AlN, there is a 2 % lattice constant mismatch. So, there is a lattice constant mismatch for epitaxial heterojunction structures grown using III-Nitride semiconductors. In addition, there is also a thermal expansion coefficient mismatch between III-Nitride semiconductors.

| | Lattice constants (\AA) | Thermal expansion coefficient (10^{-6}K^{-1}) | Melting point ($^{\circ}\text{C}$) | E_g (eV) |
|------------|------------------------------------|--|--------------------------------------|------------|
| GaN | $a_0=3.189$ $c_0=5.185$ | $3.2 \parallel c\text{-axis}$ $5.6 \perp c\text{-axis}$ | 2791 | 3.4 |
| InN | $a_0=3.54$ $c_0=5.705$ | $3.7 \parallel c\text{-axis}$ $5.7 \perp c\text{-axis}$ | 2146 | 0.89 |
| AlN | $a_0=3.112$ $c_0=4.982$ | $5.3 \parallel c\text{-axis}$ $4.2 \perp c\text{-axis}$ | 3487 | 6.2 |

Table 2.1: Property summary of III-Nitride compound semiconductor in wurtzite crystal structure [9].

2.4.Operation of LEDs

An LED is essentially a light source made from a p-n junction diode using direct band gap material that emits incoherent light. Unlike incandescent light bulbs, in which the electrical energy has to be converted to heat in a metallic filament to obtain light emission, the light emission of an LED is obtained directly from electricity via electron-hole radiative recombination. When a LED is forward-biased by applying a positive voltage to the p-type region and a negative voltage to n-type region, there is a current flow across the p-n junction, mainly caused by holes being injected into the n-type region from the p-type region and electrons being injected into the p-type region from the n-type region simultaneously [1]. When an electron on the conduction band recombines with a hole in the valence band, the electron is moving to a lower energy state, so there is an energy release during the recombination. If the recombination is radiative, a photon with energy equal to the band gap is emitted (i.e. the energy equal to the band gap is released in the form of light). Therefore, the wavelength of the light emitted by an LED due to radiative recombination is defined by the energy difference between the conduction band and the valence band [1]. This can be represented by the following approximation

$$\lambda = \frac{hc}{E_g} \quad (2.2)$$

Where c is the velocity of light, h is the Plank's constant and E_g is the band gap energy

However, radiative recombination only occurs when both energy and momentum are conserved. This means that radiative recombination does not happen frequently as the electron has to wait for the hole with the right energy and momentum to appear. The average waiting time for an electron to find a suitable hole with which to recombine radiatively is called radiative recombination lifetime (τ_r) [11]. If the semiconductor has a direct band gap structure, the bottom of the conduction band and the top of valence band occur at the same value of momentum as illustrated in Figure 2.6(a), the probability of a radiative recombination event is high in such band structure. This is because the electron in the conduction band can easily find a hole in the valence band with the same energy and momentum.

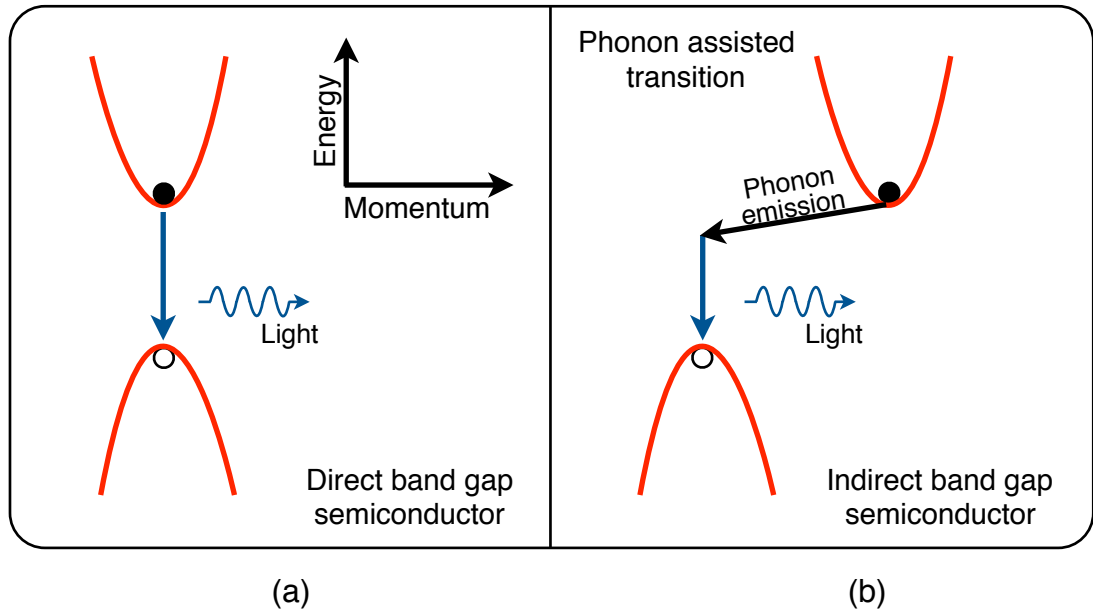


Figure 2.6: Semiconductor with (a) direct band gap and (b) indirect band gap structure.

However, electron-hole radiative recombination is not the only recombination process in a semiconductor. When a semiconductor has an indirect band gap structure, the bottom of the conduction band and the top of the valence band do not occur at the same value of momentum as illustrated in Figure 2.6(b), an electron must now undergo a change of momentum during electron-hole recombination. Conservation of both energy and momentum must be satisfied for radiative recombination to occur. Conservation of energy can easily be satisfied as the photon can take up the energy of the electron-hole pair [12], but since the photon has virtually zero momentum, the change of momentum cannot be compensated by the photon itself. Therefore, for radiative recombination to occur in a semiconductor with an indirect band gap structure, the recombination must be assisted via emission of phonons (i.e. lattice vibrations) to compensate the change of momentum, as illustrated in Figure 2.6. Such second order radiative recombination has only low probability and has a lifetime in the order of seconds [12]. This is because the electron in the conduction band has to wait for a phonon with a combined value of momentum equal to the difference between the electron and hole momentums to appear. While the electron is waiting for such phonons to appear, it can easily recombine with localised energy states in the forbidden band gap, these states are usually generated by dislocations or point defects [12]. Such recombination is non-radiative and the electron energy is converted to heat or lattice vibrations as illustrated in Figure 2.7(b). Non-radiative recombination again does not occur

instantaneously as the carrier has to diffuse to the non-radiative recombination site. The average time taken for non-radiative recombination to occur is called the non-radiative recombination lifetime (τ_n).

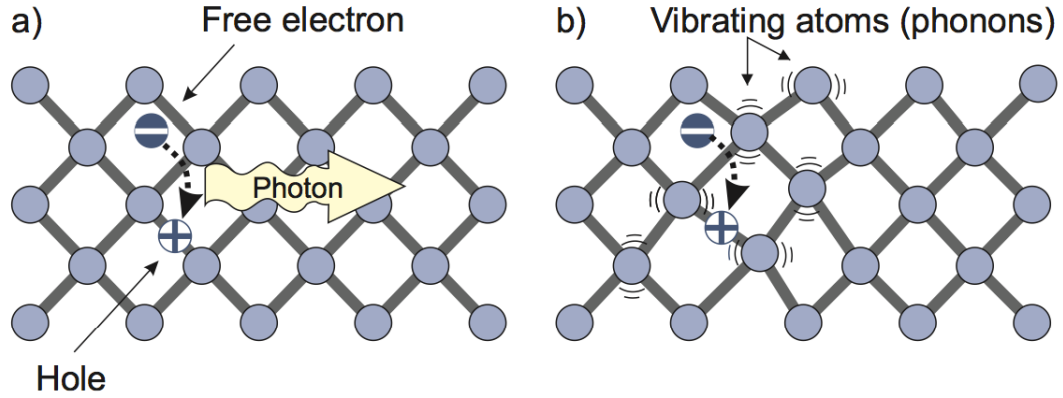


Figure 2.7: (a) Emission of photon via electron-hole pair radiative recombination.
(b) emission of phonon via non-radiative recombination [13].

An LED is a p-n junction that is designed to have a very small radiative recombination lifetime compared to the non-radiative recombination lifetime, which means the light generation process occurs very frequently with respect to the heat generation process. Internal quantum efficiency (η_i) is often used as an indicator of effectiveness of the light generation process in an LED [1]. The total recombination lifetime (τ), also known as the minority carrier lifetime. Its reciprocal defines the overall rate of electron-hole recombination, which is the sum of the rates of radiative combination (τ_r^{-1}) and non-radiative recombination (τ_n^{-1}). It is simply the sum of the radiative lifetime and the non-radiative lifetime as illustrated in equation (2.3) [1].

$$\frac{1}{\tau} = \frac{1}{\tau_r} + \frac{1}{\tau_n} \quad (2.3)$$

The internal quantum efficiency is simply given by the ratio of the number of injected carriers that recombine radiatively to the total number of injected carrier [1] as shown in equation (2.4). Therefore, τ_r in a well designed LED with high quantity low defect density material should be very small and τ_n should be very large, so that η_i is allowed to approach 100 percent.

$$\eta_i = \frac{\tau_r^{-1}}{\tau_n^{-1} + \tau_r^{-1}} \quad (2.4)$$

2.5. Layer structure of LEDs

The very first generation of LEDs only employed a simple homojunction diode structure that the p-type GaN and n-type GaN are simply put together to form an LED. When it is under forward biased condition, the majority carriers are free to widely diffuse to the opposite side of the junction. Once these carriers reach the opposite of the junction, their identities change to minority carriers and they can contribute to the recombination process over the distance of the minority carrier diffusion length (L_n). These carriers can diffuse a long distance to the opposite side of the junction as illustrated in Figure 2.8. This long diffusion length resulting in a low carrier concentration and recombination to occur over a large region [1]. According to the bimolecular equation as illustrated in equation (2.5), the radiative recombination rate (R) is proportional to product of hole and electron carrier concentrations [14]; Thus, the radiative recombination rate increases with free carrier concentration. Therefore, high concentrations of both carrier types are an essential condition to obtain high radiative recombination rate, given by

$$R = Bnp \quad (2.5)$$

where n and p are the electron and hole concentrations. B is the bimolecular recombination coefficient, which is a measure of the probability of radiative recombination (the typical bimolecular coefficient of GaN is $2.2 \times 10^{-10} \text{ cm}^3\text{s}^{-1}$) [1]

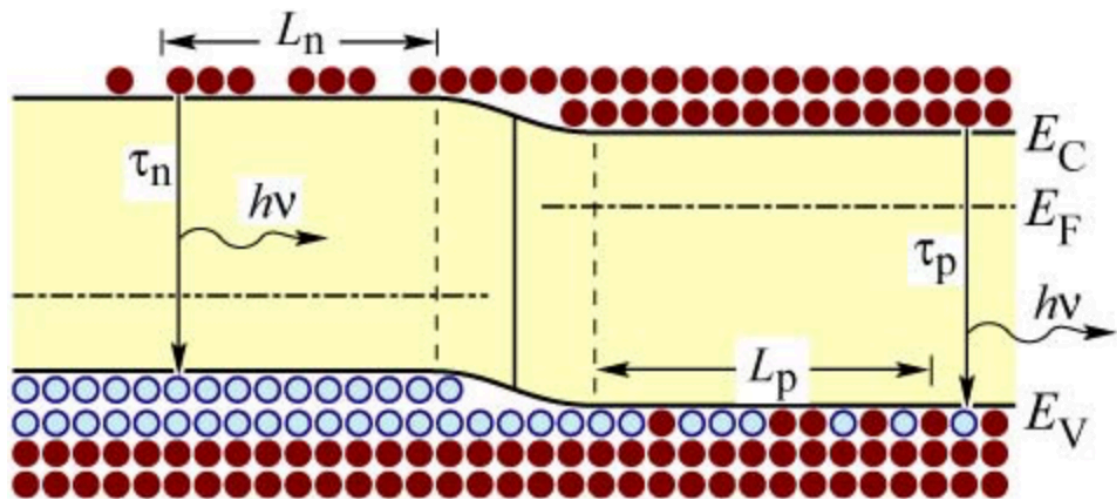


Figure 2.8: Carrier distribution of homojunction under forward biased condition [13].

The problems of low carrier concentration and recombination spreading over a large region can be resolved by using double heterojunction structure [1], which is sandwich structure made of an active region of narrower band gap semiconductor surrounded by two confinement layers of wider band gap. It is worth mentioning that the active region is where the radiative recombination occurs. When it is under forward biased condition, both electrons and holes are injected into the active region [14]. The band discontinuities at the boundaries between the wider band gap confinement layers and the active region act like a barrier to carrier diffusion and then confine the injected carriers into the active region. Such carrier confinement can significantly increase the carrier concentration in the active region. Therefore, the carrier concentration in the active region of a heterojunction structure is higher than that in a homojunction structure, leading to a higher radiative recombination rate. Figure 2.9 illustrates the schematic of a GaN based LED employing a double heterojunction structure. The confinement layers consist of p- and n-GaN, which have higher band gap energy than the InGaN active region in a typical blue or green GaN based LED. The active region is normally left unintentionally doped, so as to help inhibit carrier overflow and spill into the confinement layers.

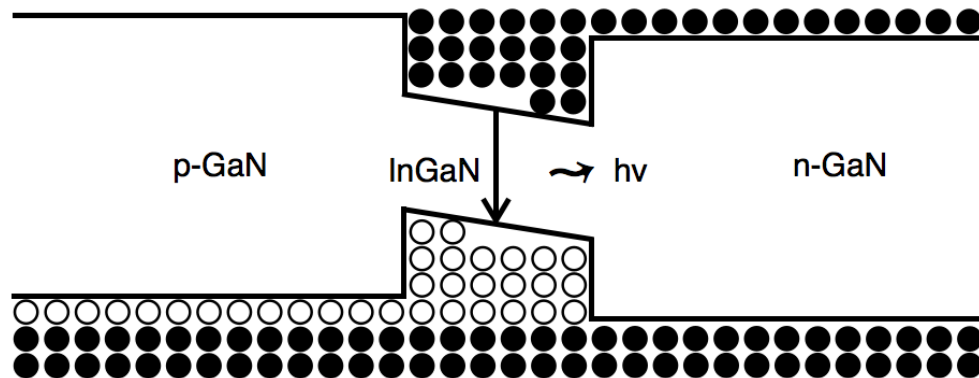


Figure 2.9: Schematic of GaN based LED using double heterojunction structure under forward biased condition.

The width of active region in a double heterojunction structure also plays an important role of confining carriers. If the width of the active region is larger than the minority carrier diffusion length, which is the average distance a minority carrier travels before it recombines [14], the carriers can also diffuse in the same way as they do in the homojunction structure. The carrier confinement

effect provided by the double heterojunction structure is reduced. Therefore, the width of active region is often made smaller than the diffusion length.

The internal quantum efficiency of a double heterojunction structure can be further improved by reducing the width of active region to the nanometer scale. When the width of the active region is reduced to nanometers, the resulting structure is also known as a quantum well. A quantum well active region allows the carriers to be further confined, resulting a higher carrier density and higher radiative recombination rates. In addition, if the active region is thin enough, the lattice mismatch between the InGaN active layer and GaN barrier layer is accommodated by pseudomorphic strain rather than having lattice relaxation occurred via the formation of dislocations [15]. It is worth noting that when the width of active region becomes less than or comparable with the De Broglie wavelength of the carrier, the energy states of the conduction band and valence band in the quantum well become discrete in the direction perpendicular to the heterojunction interfaces and no longer continuous [1], as illustrated in Figure 2.10.

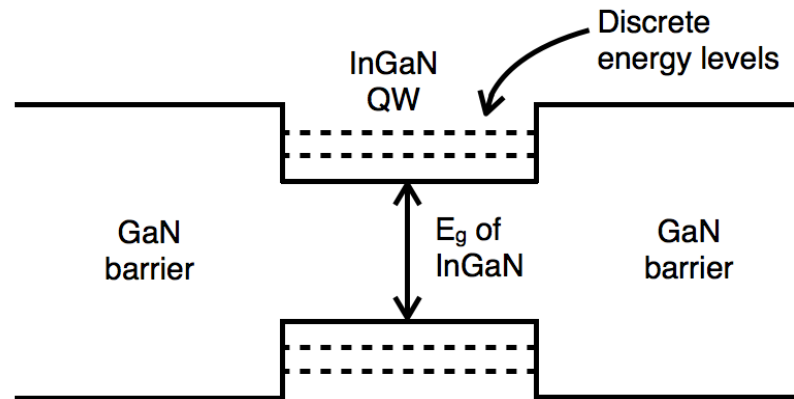


Figure 2.10: Schematic of discrete energy quantum well.

An active region comprising a single quantum well structure has a very small volume, so carriers can easily fill up the quantum well resulting carrier overflow when under high current injection condition. Any additional carriers injected into the filled up quantum well leak out of the active region and hence will not increase the light emission. Therefore, an active region often employs a Multiple Quantum Well (MQW) structure as illustrated in Figure 2.11. This structure allows the emissive volume to be increased and the overflowing carriers to be

transported to the adjacent additional quantum wells. Thus, the MQW structure can significantly enhance the light emission by allowing a higher current.

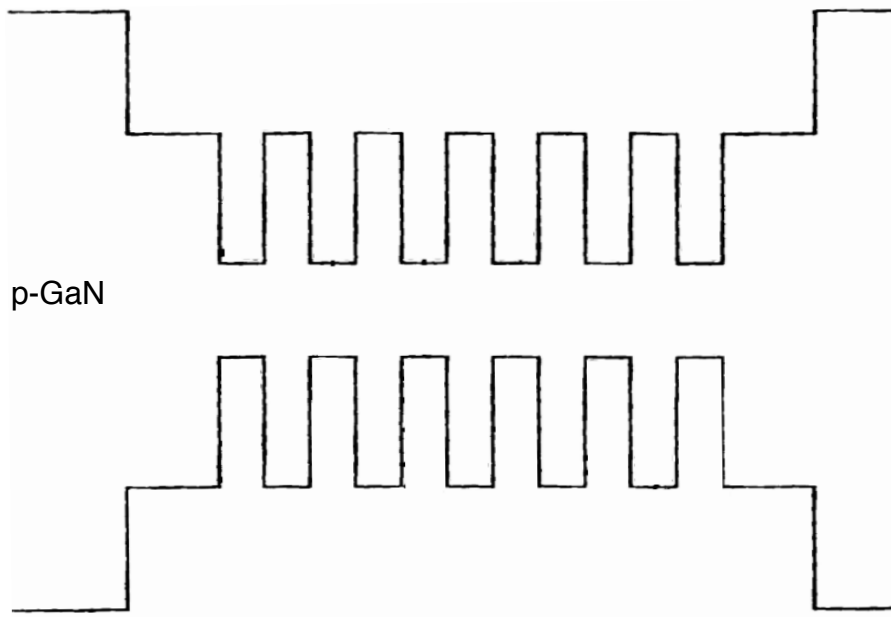


Figure 2.11: Schematic of a multiple quantum well structure [9].

Therefore, modern GaN based LEDs generally employ a MQW structure. The optimum number of quantum wells in the MQW is still a topic of investigation. However, the modern GaN-based LEDs often contain 5 to 9 pairs of MQWs [16]. The colour emission of the LED can be altered by changing the In composition rate in the InGaN active region. The higher the In content, the lower the photon energy is emitted (i.e. the light emission is red shifted with higher In content). As such, varying the In content in the InGaN active region theoretically can be used to realize red, blue and green LEDs. However, InGaN with a high In content is difficult to grow as In-rich quantum dots (clusters) are formed during the growth [7] and the lattice constant of InGaN is increasingly mismatched with that of GaN as the In content increases. Therefore, GaN based LEDs with an In-rich InGaN active region such as red LEDs are not generally used to fabricate long wavelength emitters. As a result, InGaN is generally only used for fabrications of high brightness blue and green LEDs.

2.6.References

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Chapter 3

Device Fabrication and Experimental Techniques

3.1. Fabrication of GaN on Si Vertical LEDs

In this chapter, the fabrication procedures of VLED samples and the techniques used in their characterization are described. The fabrication process of GaN on Si VLEDs is very challenging as it involves wafer bonding the LED wafer to a foreign substrate and removing the original Si growth substrate. Compared to GaN LED epitaxy grown on sapphire, inappropriate fabrication process can readily lead to cracking of the LED epitaxy layer during wafer bonding and after the removal of original Si growth substrate. Also, the bonding metal, in particular, is vulnerable to chemical attack during subsequent processing.

All the InGaN/GaN LED epitaxy was grown on a Si substrate with orientation of [111] by metallorganic chemical vapour deposition (MOCVD) obtained from Plessey Semiconductor Limited. The emission wavelength of the LED wafers supplied was 470 nm. The LED wafers had 200 nm thick multiple quantum wells (MQWs) stack as the active region with ~3 nm quantum wells. The 90 nm thick super lattice layer serves as a strain management layer. The n-type and p-type confinement layers were 1.47 μm and 95 nm thick respectively. A thin AlGaIn layer, 22 nm, between the p-type confinement layer and the MQW acted as an electron blocking layer, which prevents electrons from escaping the MQWs. A 650 nm of AlGaIn serves as a buffer layer and a 200 nm of AlN as the nucleation layer. The details of the LED wafers are illustrated in Figure 3.1.

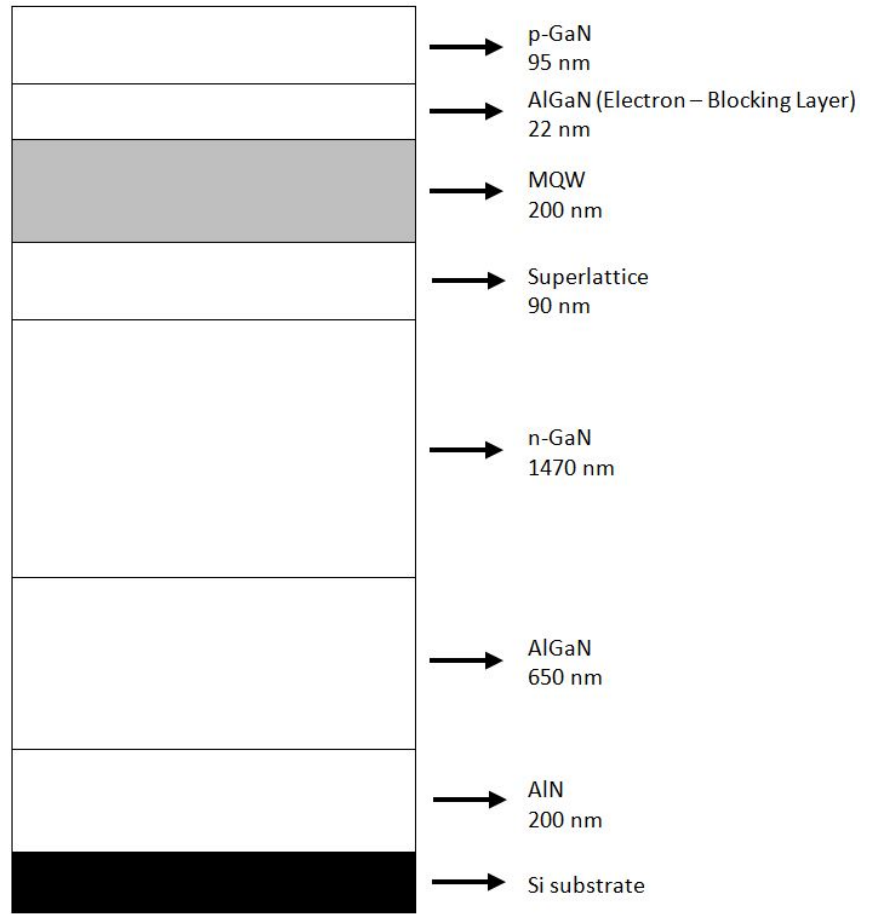


Figure 3.1: Layer structure of GaN on Si LED Wafer.

Figure 3.2 shows a flow chart of the overall fabrication process used in making the VLEDs. Briefly, the fabrication process is first started with pixelating the LED wafer into isolation islands by inductively coupled plasma (ICP) etching. The pixel size was $\sim 1 \times 1$ mm and comprised a single device of approximately the same area. SiO_2 is then deposited on to the side walls of the islands of the pixelated LED wafer and followed by the p-type ohmic contact and bonding metals depositing on top of the pixelated LED wafer. The LED wafer is then held in contact with a similarly metalized Si carrier substrate under high pressure nitrogen in the wafer bonder for wafer bonding process. Subsequently, the original Si growth substrate on the wafer bonded sample is removed by a combination of mechanical lapping and SF_6 plasma. The high band gap material of AlGaIn and the undoped GaN buffer layer are then etched away to expose the N face n-GaN for the n-type contact deposition by electron beam evaporator (EBE). Each key process involved in the fabrication of complete vertical light emitting diodes (VLEDs) is described in detail in the following section.

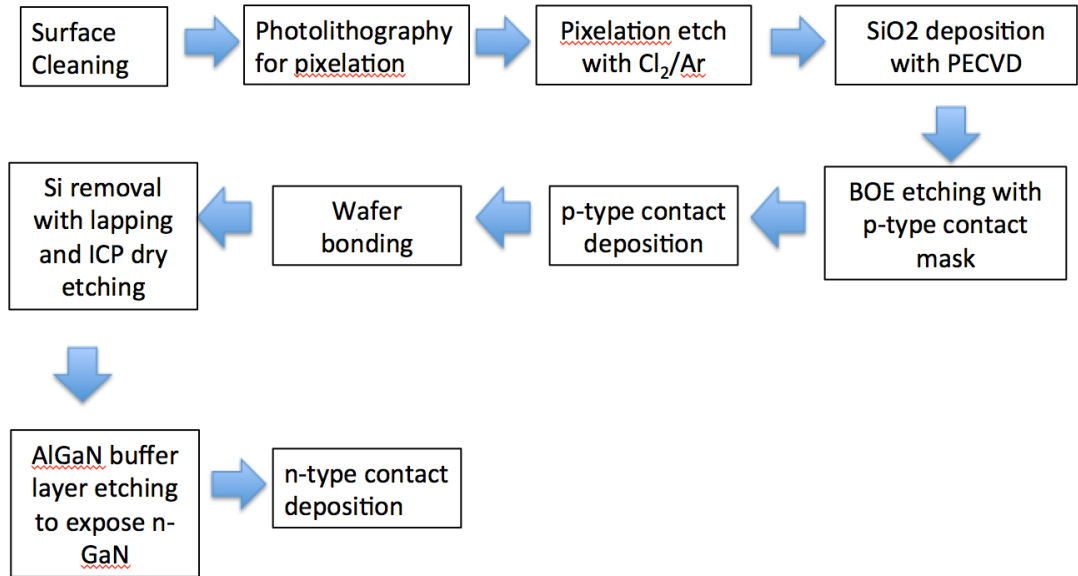


Figure 3.2: The flowcharts of fabrication processes of VLED device.

3.1.1.Surface Cleaning

Although the wafer samples are stored with great care in a sample box, it is inevitable they become contaminated during handling. As a result, the surface of the wafer is first cleaned with acetone and followed by iso-propyl alcohol (IPA) before the application of photoresist for the first level mask used to define the pixels. The use of acetone ensures that most of organic contaminants are removed. Since acetone cannot be dissolved in water, IPA is used to clean off any residual acetone on the surface. The wafer is then rinsed with deionized water (DI water) and then blown-dried with nitrogen.

3.1.2.Photolithography of Pixelation Pattern and Etch

Photolithography is a process, which transfers a designed pattern on a mask to a UV-light sensitive photoresist by shining UV-light through the mask. Photoresist is an organic compound and its solubility can be changed by exposing it to UV-light. For instance, when a positive resist is exposed to UV-light, the exposed part of the positive resist becomes soluble in a developer and can then be removed by the developer. The designed pattern, such as electrodes or a test structure, is printed on the mask. So when UV-light is shone

on the mask, some of the UV-light is blocked by the pattern. The transmitted UV-light is able to go through the mask and exposes on the photoresist. This light then transfers the pattern on the mask to the photoresist by changing the solubility of the unwanted parts which are then removed using a developer.

Prior to the application of photo-resist, the wafer sample was heated on a hotplate at 100 °C for 1 minute, in order to remove any remaining moisture. After the baking, the wafer was transferred to the spinner for photoresist coating. A positive photoresist, S1828, was used for the pixelation patterning. After dispensing the S1828 resist on to the surface of the wafer, the sample was then spun at 3000 R.P.M. for 30 seconds with an acceleration of 10000 R.P.M. to form a 3.5 μm thick photoresist film. After coating the sample with photoresist, a 3 minute soft-baking on a hotplate at 115 °C was performed. This was to remove the solvent in the photoresist and increase its hardness as well as adhesion to the wafer.

After the 3 minute soft-baking, the sample was ready for photolithography. The photoresist coated sample was placed on a mask aligner and then brought in contact with a pixelation pattern mask. The process was carried out on fragments taken from 150 mm diameter wafers. Whilst the starting wafers were often bowed in a regular way, due to the lattice constant and coefficient of thermal expansion (CTE) mismatches of GaN and Si, the curvature of the fragments was often more varied. This made the epitaxy more vulnerable to cracking during sample handling and wafer bonding. This problem was resolved by pixelating (partially etching through) the epitaxy. The remaining n-GaN can act as a barrier layer to protect the subsequent SiO₂ passivation layer from being etched by the Si growth substrate etchant in the growth substrate removal process. A mask aligner is used to align the pattern on to a desired position on the sample and expose UV-light. To transfer the pattern on to the photoresist, the wafer was exposed to UV light for 150 mJ/cm dose. The sample was then put into a 351 developer for 1 minute after UV exposure to remove the unwanted photoresist. Figure 3.3 shows the schematic of the pixelation pattern and an illustration of exposing a positive photoresist.

After the pixelation pattern transferred onto the photoresist, the sample is then put into the Oxford Plasma System ICP100 to etch 1600 nm to create 1 mm² square islands in Cl₂/Ar (10 sccm/100 sccm) plasma. This reduced the pre-existing curvature caused by tensile stress in the GaN caused by the lattice and CTE mismatch.

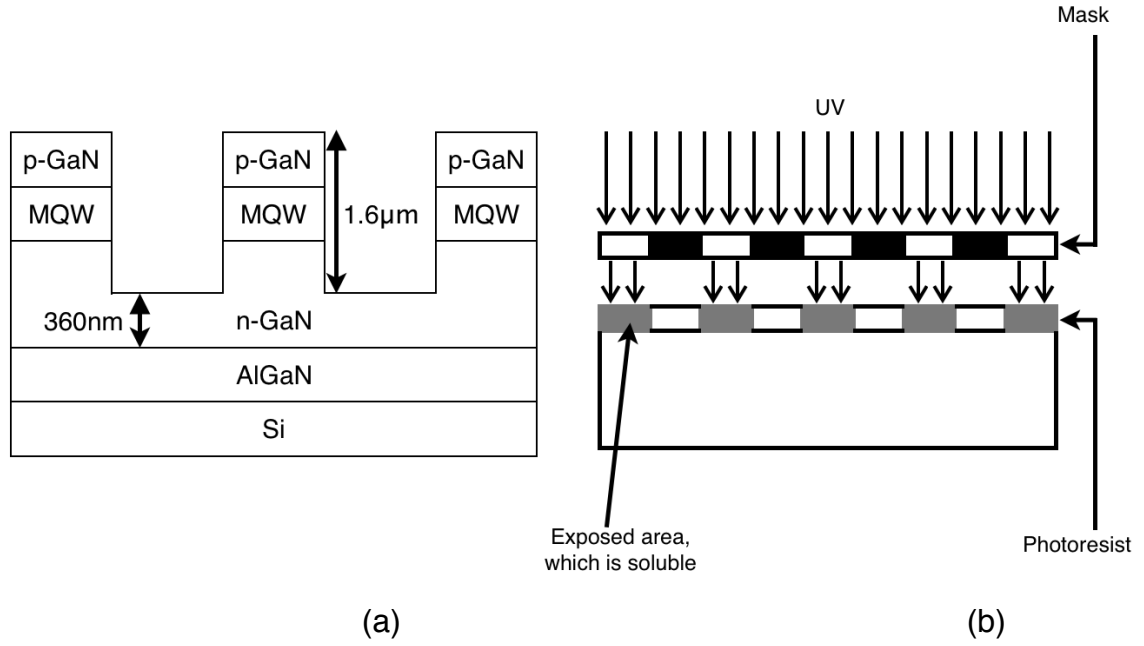


Figure 3.3: Schematic of pixelation pattern on (a) LED wafer the mask and (b) a positive photoresist is being exposed to UV light.

3.1.3. Photolithography for p-Type Contact Mask and CTLM

After the GaN etch, the remaining photoresist was removed by using 1165 photoresist remover. Prior to the p-type contact pattern and metal deposition, 300 nm of SiO₂ was deposited on to the whole LED wafer using Plasma Enhanced Chemical Vapour Deposition (PECVD). This SiO₂ is to prevent bonding metal from being deposited to the sidewall and the n-GaN as illustrated in Figure 3.4, causing short circuit problem during wafer bonding process.

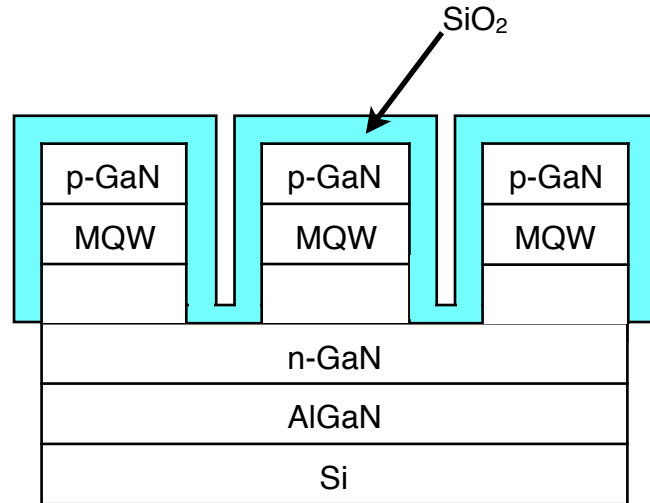


Figure 3.4: Schematics of SiO₂ insulating the LED side wall and n-GaN.

After the SiO₂ deposition, the LED wafer was patterned with the p-type contact for device fabrication using photolithography. The procedure for photolithography is the same for pixelation pattern photolithography except for the fact that p-type contact mask pattern requires a negative photoresist (nLOF AZ 2070), which is designed for pattern definition by lift-off with undercuts. The negative resist has an opposite chemical property to the positive resist, so the unexposed parts of the photoresist are soluble and are removed in the developer. Figure 3.5 shows schematically the principle of the lift-off process. The schematic of the p-type contact pattern is illustrated in Figure 3.5(a), the purpose of this pattern is to allow metal only deposited on to the area with the blank white area and the edge of the LED device is protected. It can be seen that metal can only be deposited on to the area without photoresist as seen in Figure 3.5(c). When the photoresist is dipped into a resist stripper the undercut of the photoresist allows the stripper to be able to dissolve the resist easily.

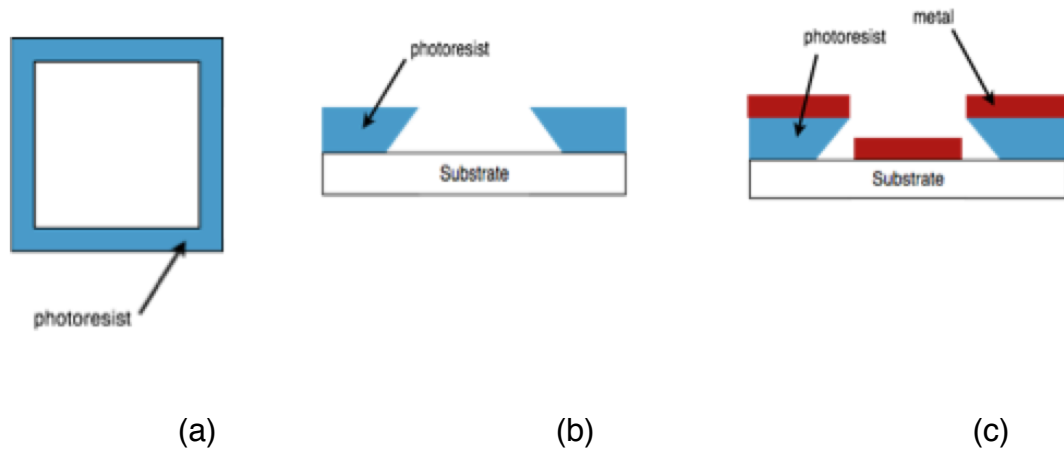


Figure 3.5: Schematics of (a) p-type contact pattern, the blue area represents the photoresist and the white area represents the LED epitaxy, (b) photoresist with undercut for the ease of lift-off and (c) metal deposited on top of photoresist and on the LED epitaxy layer.

3.1.4. Metallization For p-Type Contact

After a buffered oxide etch (BOE), which comprised of 5 part of ammonium fluoride to 1 part of 49 % of HF in water. In order to pattern the LED wafer with the p-type contact pattern, the sample was put into buffered oxide etch (BOE), which comprised of 5 part of ammonium fluoride to 1 part of 49 % of HF in water, for 5 minutes, to remove SiO_2 to expose the p-GaN for p-type metal. After removing the insulating oxide, the sample was put into $\text{HCl}:\text{H}_2\text{O} = 1:1$ for 5 minutes, so as to remove any Ga droplets and Ga_2O_3 on the surface. After the 5 minute dip, the sample was rinsed with DI water and blow-dried using nitrogen. Subsequently, the sample was immediately loaded into the Edwards auto 306 Electron Beam Evaporator (EBE) for p-type contact metal deposition. The chamber was pumped down to 3×10^{-6} mBar before commencing the metal deposition, so as to ensure that the chamber was virtually free of oxygen and moisture. After metal deposition (metals detailed in Chapter 4), the wafer was put into resist stripper (Microposit 1165) for 10 minutes to lift-off the unwanted metal by dissolving away the photoresist mask. During the lift-off process, the sample was put into a basket, so that it was perpendicular to the bottom of the beaker. This was to ensure that the lift-off metal would not re-deposit on to the sample. Figure 3.6 illustrates the p-type contact metal deposited on to the LED

wafer. Schematics of p-type contact pattern, the grey rectangular boxes represent the p-type metal and blue area represents the SiO_2 layer.

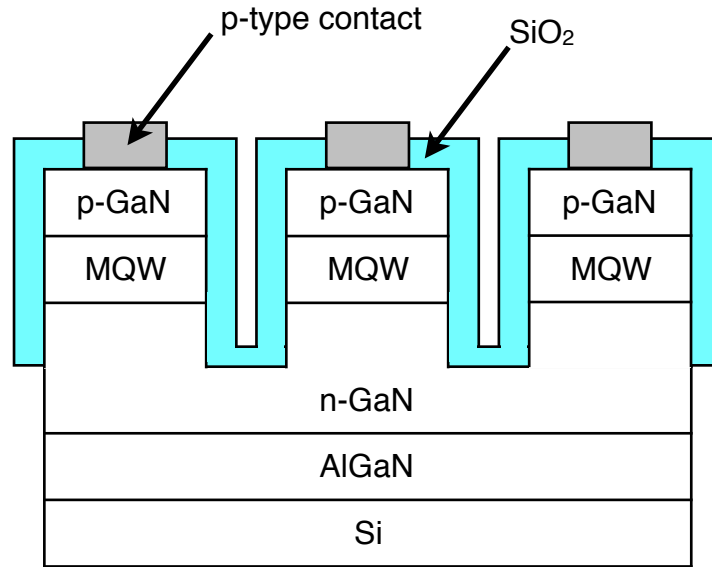


Figure 3.6: Schematic of p-type metal deposited on p-GaN after the SiO_2 etch.

3.1.5. Rapid Thermal Annealing

After defining the p-type contact area, the LED and any p-GaN test samples were annealed in an oxygen ambient for 2 minutes using a Rapid Thermal Annealer (RTA). This thermal treatment is critical for obtaining a good p-type ohmic contact and will be discussed in detail in Chapter 4. A rapid thermal annealer is designed to ramp up to a high temperature and then cool to room temperature in a short period of time and is a technique often used in ohmic contact formation to achieve optimum alloying of the metals with the semiconductor without excessive in-or-out diffusion.

3.1.6. Wafer Bonding and Lapping

The wafer bonding process is probably the most critical step during the VLED fabrication process. This allows the LED epitaxy to be bonded on to a new carrier substrate with a reflective p-type ohmic contact inserted and the original growth substrate to be removed, so that the emitted light can be extracted rather than being absorbed in the silicon. After the p-type contact deposition, the bonding metal stack, typically Ti/Ni/Sn/Au (200 nm/100 nm/1700 nm/50 nm) and

Ti/Pt/Ag/Au (200 nm/100 nm/3500 nm/50 nm) was deposited on the LED wafer and Si carrier substrate using the EBE, respectively. The Ti layer is served as an adhesion layer to the Si carrier and to p-type reflective metal contact on the LED epitaxy. The Ni layer is used as an under bond metal layer to connect the solder to the adhesion layer. The Au layer on top of both bonding metal stack is deposited to prevent the Sn and Ag from oxidation, while the Ni, Sn and Ag in the stack form a bonding solder, which bonds the LED epitaxy to the Si carrier substrate. The sample and carrier substrate are mounted on a heated graphite pedestal inside a vacuum tight chamber, with a tight-fitting but sliding plunger placed on top. the lower section of the chamber is then evacuated to a pressure of 6 MPa to put the plumber down on to the sample-carrier substrate stack, pulling them slowly together. There is a gas inlet in the top section of the chamber to optionally increase the pressure on the sample and carrier substrate to force them into intimate contact.

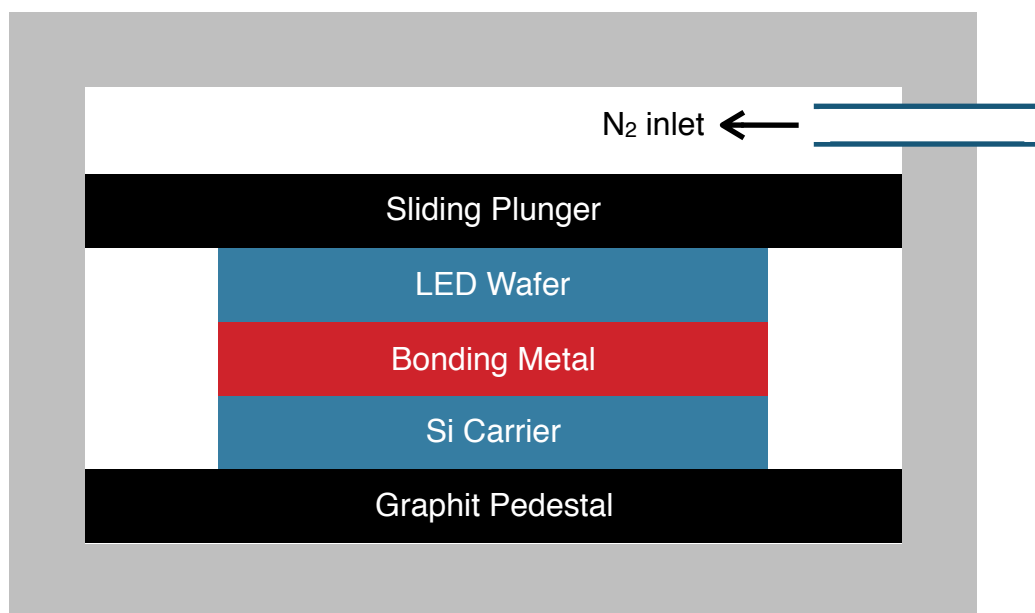


Figure 3.7: Schematics of wafer bonder with optional N_2 inlet and a heated graphite pedestal.

The bonding process is carried out in vacuum, at the pressure of 6 MPa, to prevent the bonding metal from oxidation. The chamber is then heated to 260 °C and held for 30 minutes for bonding to take place. The Sn bonding metal starts to melt at approximately 232 °C during the temperature ramping process [1], When the chamber temperature reaches 260 °C, the melted Sn will react with the thick Ag layer deposited on the LED side forming an intermetallic

compound of Ag_3Sn . The melted Sn will also react with the Ni layer underneath forming an intermetallic compound of Ni_3Sn_4 . Figure 3.8 illustrates the SEM image of resultant joint of the LED epitaxy bonded to a Si carrier substrate. It can be clearly seen under EDX data that the resultant joint is made of Ag_3Sn , Ni_3Sn_4 and a Ag-Sn solid solution, and is usually free of large voids.

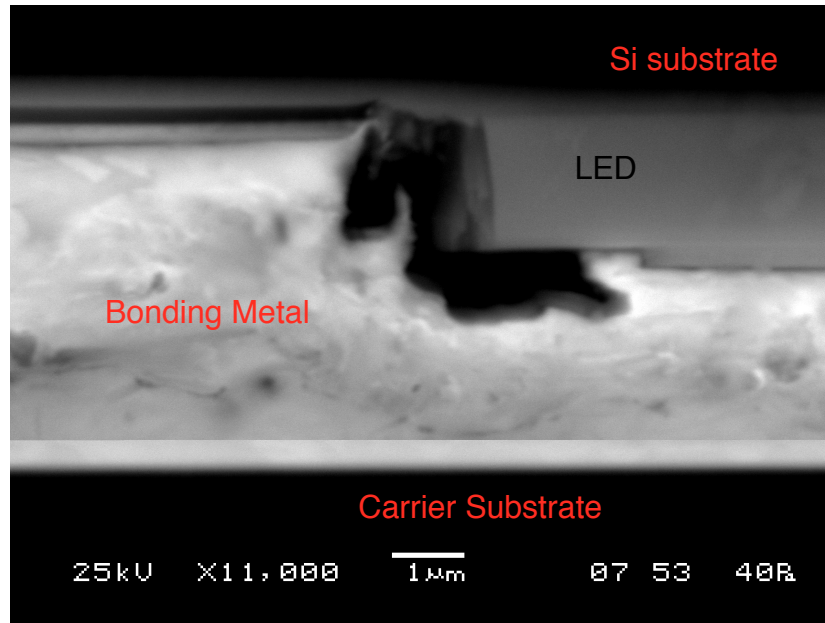


Figure 3.8: SEM image of the resultant wafer bonding joint of GaN-on-Si VLED.

After the LED epitaxy has been bonded to a Si carrier substrate, the thickness of original Si growth substrate was reduced to approximately $100\ \mu\text{m}$ by mechanical lapping process and the remaining Si was then removed by SF_6 plasma etching.

3.1.7. AlGaIn removal and n-type Contact deposition

After the Si growth substrate being removed, the AlN nucleation and AlGaIn strain buffer layers were etched in Cl_2/Ar (20 sccm/50 sccm) inductively coupled plasma (ICP) etching at 100 W RIE power and 1000 W ICP power to expose the n-GaN. The n-type contact pattern was defined using photolithography technique described in section 3.1.4. The standard n-type contact metal of Ti/Al/Ni/Au (20 nm/60 nm/20 nm/100 nm) was then deposited using E-beam evaporation and lifted off using 1165 resist stripper as illustrated in Figure 3.9.

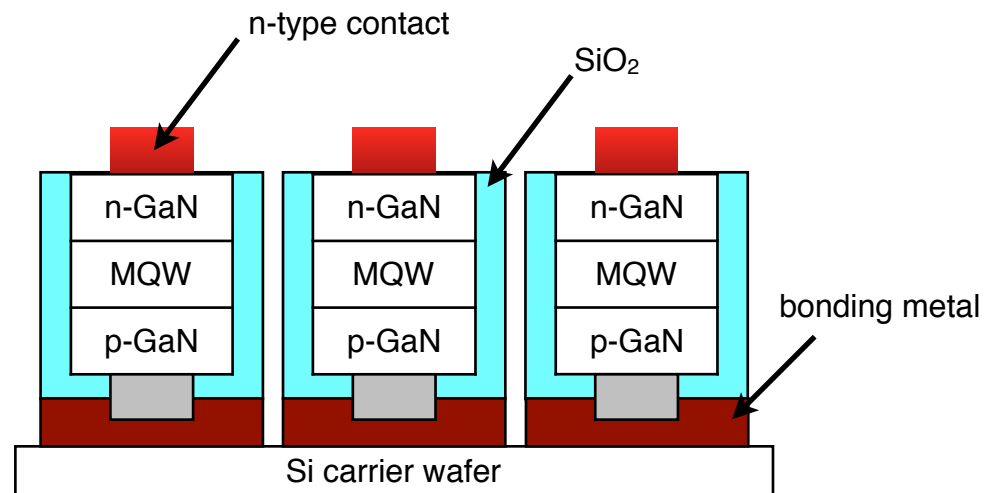


Figure 3.9: Schematics of a completed vertical LED.

3.2. Inductive Coupled Plasma Etcher

In general, dry etching is performed by ionizing a gas to create ions, which react with the target material. In other words, it is done using a plasma or etchant gases to remove the unwanted material on the sample. The etching mechanism in a dry etch process is categorized into three types - high kinetic energy ions (physical dry etch), chemical reaction (chemical dry etch) and the combination of both physical and chemical etch (reactive ion etch).

Physical Dry Etch

In a physical dry etch process, there are no chemical reactions involved during the etch. It is purely done by using ions to bombard the material surface. In other words, high kinetic energy particle beams are used to knock off the atoms from the target as illustrated in Figure 3.10. It is worth noting that the etch is usually anisotropic and both the unmasked and masked unmasked material is removed [2]. However, the etch rate of a physical dry etch process is generally very slow. Further, since both target and mask materials are removed, often at quite similar rates, this dry etch process has clear implications on the design of the etch mask and the etch depths that can be achieved.

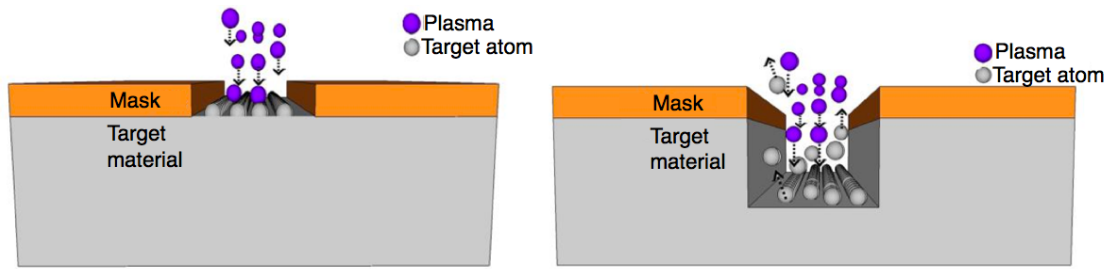


Figure 3.10: Schematics of physical dry etch in which plasma hits the target material with high energy to remove the material atoms [2].

Chemical Dry Etch

In chemical dry etching, the etch is purely performed by chemical reaction between the etchant gas and material, so the etch can be very selective. There are no physical mechanisms involved. The chemical dry etch is usually isotropic and undercut is inevitable (i.e. vertical wall is hard to achieved), unless due to the by-prudcts of the chemical process is non-volatile and does not react with the active etchant species. Figure 3.11 illustrates the etch profile of an isotropic etch with a Si substrate.

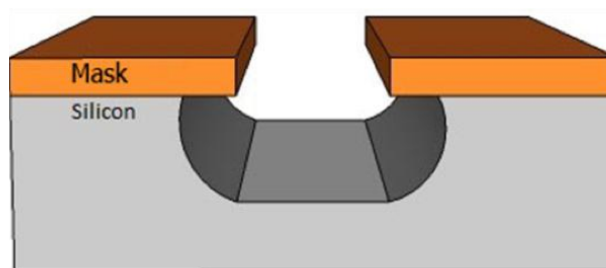


Figure 3.11: Isotropic etch profile as a result of chemical dry etch [2].

The etch rate can either be fast or slow depending on the etch conditions, for example the chamber pressure, temperature and etchant to be used.

A plasma etcher is designed for chemical dry etching. The reaction chamber is usually kept under mTorr range and has two electrodes - one at the top of the chamber and the other one at the bottom. The top electrode is generally fitted with a Radio Frequency (RF) source to create plasma. The gas inlets are normally located next to the RF source as illustrated in Figure 3.12. The sample is placed on the bottom electrode, which is connected to ground.

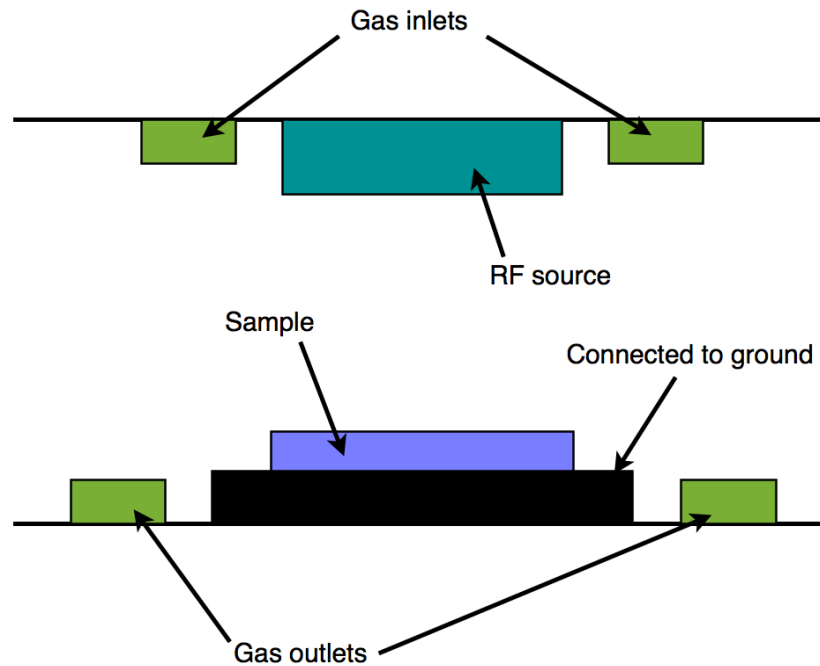


Figure 3.12: Schematics of the reaction chamber of a plasma etcher.

The plasma etch process is started by evacuating the chamber to mTorr range and the etchant gas is then introduced into the vacuum reaction chamber. This etchant gas is ionized by the RF source. The resulting ions can move randomly in the reaction chamber, when they diffuse onto the surface of the sample, the ions will form what should be a volatile chemical compound with the atoms of the target material, which are then removed by the vacuum pumping system. It is worth knowing that If the etch by-products are not sufficiently volatile, a chemically inert species like Argon is often added to the gas stream to sputter them away. The consequence of non-volatile, non-reactive by-products and Argon ion sputtering is that the sidewalls of an etch feature can become coated with the by-product while the material being etched remains exposed to the etchant at its base. This results in highly anisotropic etching.

Reactive Ion Etch

Dry etch can also be performed using both the physical and chemical dry etch mechanisms, at the same time and this etch process is called Reactive Ion Etching (RIE). In RIE, there are three etch mechanisms. First, the ions hit the material surface and knock off the target material atoms. Second, the ions diffuse onto the material surface and form a volatile chemical compound, which is then pumped away. Third, the ions first accelerate to hit the sample and form a volatile compound, which is then pumped away. Since RIE is a combined process, the etch rate is usually very fast and the etch species and conditions chosen to yield anisotropic etching.

The reaction chamber of RIE etcher is very similar to plasma etcher reaction chamber. The RIE reaction chamber again has electrodes at the top and bottom of the chamber. The top one is connected to the RF source and the bottom one is connected to DC bias voltage via a capacitor. The etchant is introduced into the chamber through the gas inlet at the top, the RF is used to ionize the etchant to produce ions and electrons. Since a capacitor is placed in between a RF source and the bottom plate, the electrons accumulate on the surface of sample sitting on top of the bottom electrode. The electrons adsorbed on the surface of sample make the sample negatively charged. The resulting potential difference between the plasma and the negatively charged electrode is called self-biased (V_b) [3]. This sets up an electric field that causes the positively charged etchant ions accelerate to hit the sample and then form mostly volatile compounds that are pumped away. Figure 3.13 illustrates the operation of RIE reaction chamber. It is worth noting that the higher the chamber pressure the higher the etch rate. This is because higher pressure increases the chance that the ions are in contact with the sample [3].

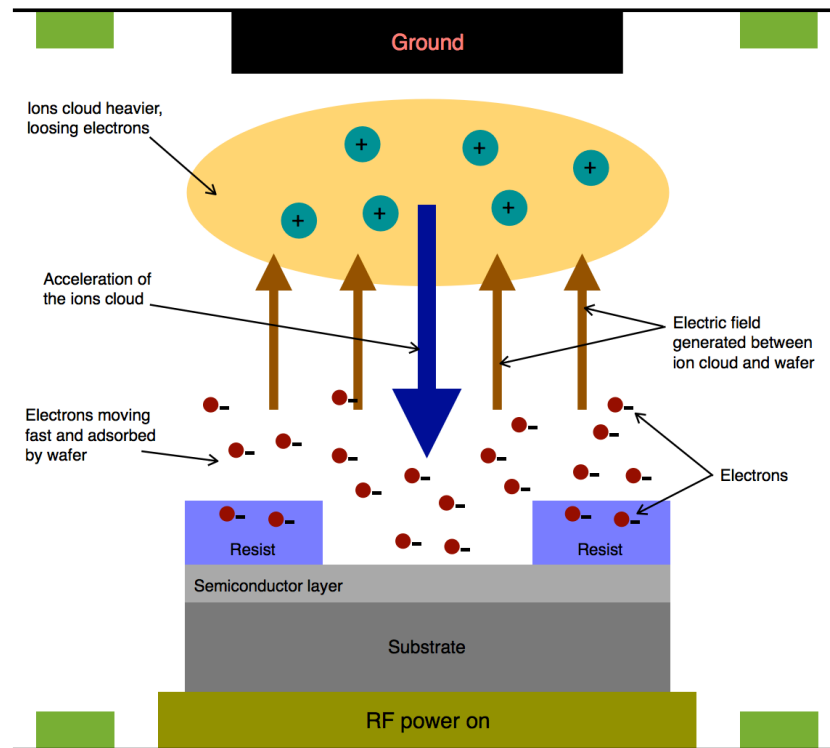


Figure 3.13: The Schematic of electrons adsorb on the surface of sample.

There are two main advantages of using RIE: the first one is that the etch rate is improved by the additional physical dry etch mechanism. The target material atoms are knocked off by the ion bombardments. The second advantage is that the ions have greater chance to move in the direction of sample as electrons adsorbed on the surface of sample set up an electric field that accelerates the aggressive ions towards the substrate being etched. Figure 3.14 illustrates the etching mechanism during RIE process.

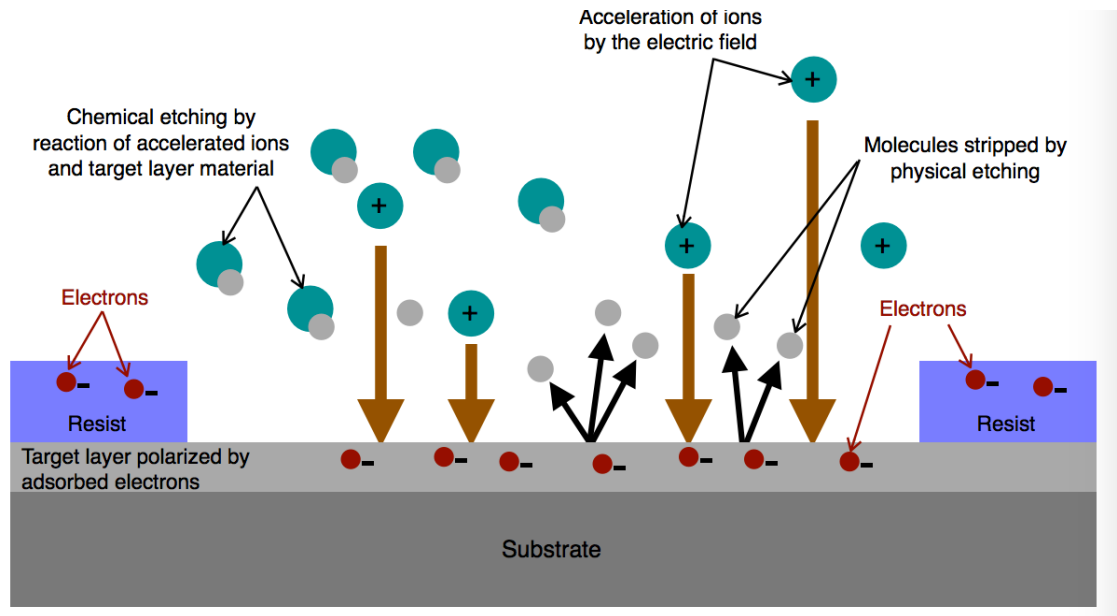


Figure 3.14: Demonstration of chemical dry etch assisted by physical dry etch.

GaN etching is among the most important step amongst all the process steps used in making the VLEDs and test structures and great care must be taken. This is because if the unwanted undoped AlGaN buffer layer is not completely removed during etch, the n-GaN is not exposed. As a consequence, the n-type contact cannot be deposited on the n-GaN after the original Si growth substrate resulting a high contact resistivity.

An Oxford Plasma System ICP 100 etcher was used to perform the GaN etch in this work. ICP etcher stands for Inductively Coupled Plasma etcher. It operates with the same principle as the RIE etcher except for the fact that there are inductive coils connected to RF source surrounding the top of chamber as an additional plasma generator to increase the plasma density and a RF, low frequency or DC bias voltage is connected to the substrate holder via a capacitor to increase the ion bombardment on the sample, as illustrated in Figure 3.15. Therefore, the etch rate for an ICP etcher is a lot faster than that for a traditional RIE etcher.

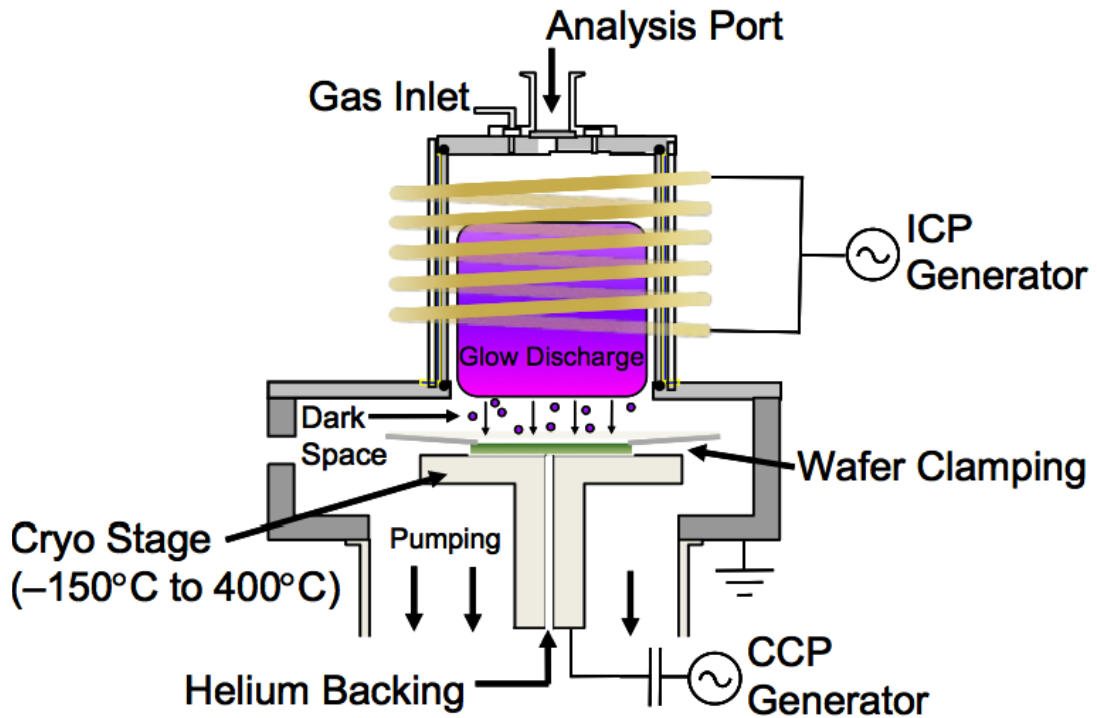


Figure 3.15: Schematic of ICP etcher reaction chamber [4].

The Oxford Plasma System ICP100 has two chambers - the load-lock chamber and a reaction chamber. The reaction chamber has two RF sources as shown in figure 3.15 - one is connected to the substrate at the bottom of the chamber, known as RIE RF source. The other one, which is to enhance the plasma density, is connected to the coils surrounding the top of the chamber, known as ICP RF source. Therefore, the ICP etcher has two RF power sources - The RIE RF power affects the etchant ion energy: So if the RIE power is increased the ions are more energetic. This leads to stronger ion bombardments. While the ICP power affects ion density in the chamber: the higher the ICP power the higher the ion density, but the magnitude of ion bombardment stays unchanged. Thus, increasing both the ICP and RIE power can cause an increase in the etch rate. However, it is intuitively clear that the increase in the etch rate is relatively smaller by increasing the RIE power compared to that by increasing the ICP power. This is because the etch rate of physical dry etch (ion bombardment) is low.

After the sample is transferred to the reaction chamber via the load-lock chamber, the etchant gases, Ar and Cl (Ar/Cl), are introduced into the reaction

chamber through the gas inlets. The RF sources are then used to ionize the Ar and Cl gases to produce positive ions and to create electrons. As described above, since the electrons are far more lighter than ions, they have a greater chance to be in contact with the sample and adsorb on the surface of sample. The electrons adsorbed on the surface of the sample then made the surface negatively charged, which attracted the positively charged Ar and Cl ions. As a result, the Ar ions are accelerated towards the sample direction and knock off the nitrogen atoms. The Cl ions are also accelerated to hit the GaN surface and then the Cl ions react to form GaCl with Ga atoms, which is volatile and pumped away by the vacuum system. The etch rate of ICP etching is a lot faster as the ion density is a lot higher. Figure 3.16 demonstrates the etching mechanism of GaN etch.

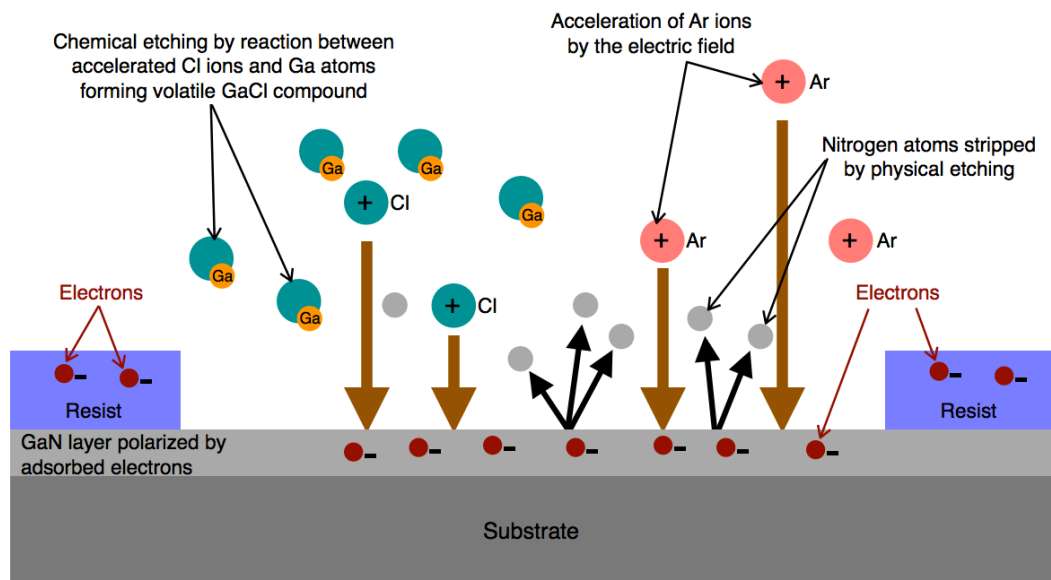


Figure: 3.16: Illustration of etch mechanism during GaN etch.

3.3.Circular Transmission Line Model

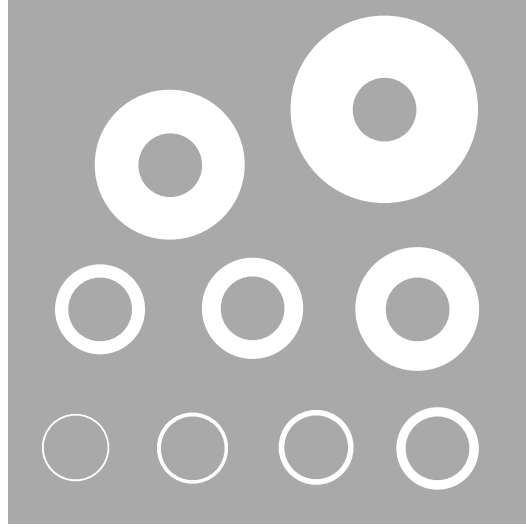


Figure 3.17: Test structure of circular transmission line model.

The specific contact resistivity (ρ_c) cannot be measured directly and can only be extracted from measurements of the current-voltage (I-V) characteristics of metal contact test structures. The geometry of these metal contact test structures can be rectangular or circular depending on the model. The most popular approach to extract specific contact resistivity is the Circular Transmission Line Method (CTLM), which models the contact between a metal and a semiconductor as a resistive network [5, 6]. This method involves depositing a large rectangular contact metal on the semiconductor layer to fabricate the test structures. Within the test structure, there are nine circular cutouts with different radius (r_o) with circular test contact pads of fixed radius (r_i), located at the centre of each circular cutout with various separation distances (d). Figure 3.17 illustrates the CTLM test structures used for this work. The spacing between these nine test cutouts and test contact pads are 3, 5, 10, 15, 20, 30, 50, 85 and 120 μm .

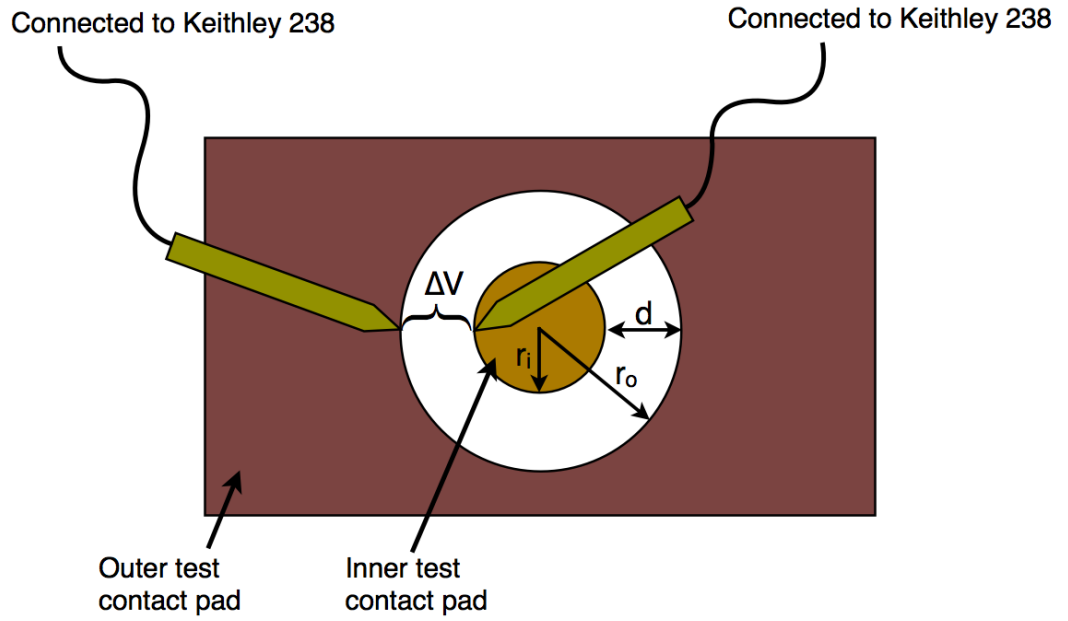


Figure 3.18: Demonstration of measuring the resistance between the contact test cutout and the circular test contact pad.

If a two point probe method is used, a current (i) is applied between the large metal contact surrounding the cutout and the circular test contact pad. There is a voltage drop (ΔV) across the spacing (d) as illustrated in Figure 3.18. The voltage drop across the spacing can be represented by the following equation [6]:

$$\Delta V = \frac{iR_s}{2\pi} \left[\ln \left(\frac{r_o}{r_i} \right) + \frac{L_T I_o \left(\frac{r_i}{L_T} \right)}{r_i I_1 \left(\frac{r_i}{L_T} \right)} + \frac{L_T K_0 \left(\frac{r_o}{L_T} \right)}{r_o K_1 \left(\frac{r_o}{L_T} \right)} \right] \quad (3.1)$$

Where i is current flowing through the spacing, R_s is the sheet resistance of semiconductor, L_T is transfer length, I_o , I_1 , K_o , K_1 are Modified Bessel Functions of first and second kind, r_o is the radius of circular cutout, r_i is the radius of inner circular contact pad.

The transfer length (L_T), which is also known as the effective contact area, is the average distance that current travels in the semiconductor under a metal contact before it falls to $1/e$ of its value at the input contact. It can be represented by the following equation:

$$L_T = \sqrt{\frac{\rho_c}{R_s}} \quad (3.2)$$

Under the condition where both r_i and r_o are greater than L_T by at least a factor of 4, both I_o/I_i and K_o/K_i are approximately equal to unity [6]. Thus, equation (3.1) becomes:

$$\Delta V = \frac{IR_s}{2\pi} \left[\ln \left(\frac{r_o}{r_i} \right) + L_T \left(\frac{1}{r_i} + \frac{1}{r_o} \right) \right] \quad (3.3)$$

Where equation (3.3) can be written in terms of spacing (d)

$$\Delta V = \frac{IR_s}{2\pi} \left[\ln \left(\frac{r_i + d}{r_i} \right) + L_T \left(\frac{1}{r_i} + \frac{1}{r_i + d} \right) \right] \quad (3.4)$$

The resistance (R_T) between the circular cutout and the inner circular contact pad is the voltage drop across the spacing divided by the current flowing between the two contact pads. So it can be written as the following equations:

$$R_T = \frac{\Delta V}{I} \quad (3.5)$$

$$R_T = \frac{R_s}{2\pi} \ln \left(\frac{r_i + d}{r_i} \right) + \frac{\sqrt{R_s \rho_c}}{2\pi} \left(\frac{1}{r_i} + \frac{1}{r_i + d} \right) \quad (3.6)$$

It can be seen from the above equation that the first term represents the resistance contributed from the semiconductor material and the second term represents the resistance contributed by the cutout metal contact and the inner metal contacts.

Therefore, if a constant voltage (V) is applied to the inner and outer (cutout) test contact pads with spacing (d) as illustrated in Figure 3.17 and the current flow between them (I) is measured, the resistance (R_T) between the pads can be calculated. By repeating this I-V measurement for all nine pairs of inner and cutout contact pads with different spacing distances, the resistance between each pair of circular test pads can be obtained from the corresponding I-V data measured. The resistances of these nine pair of contact pads are then plotted against their corresponding outer radius ($r_o = r_i + d$). Since r_i is constant for all

nine CTLM test structures on the p-contact with only r_o varying due to the change of spacing distance (d), which is a known variable. R_s and ρ_c can then be calculated by fitting the resistance data to equation (3.6) using the least square method (i.e. varying trial values of ρ_c and R_s to fit the measurements to the equation. Figure 3.19 illustrates an example of extraction of the specific contact resistivity by using curving fitting method.

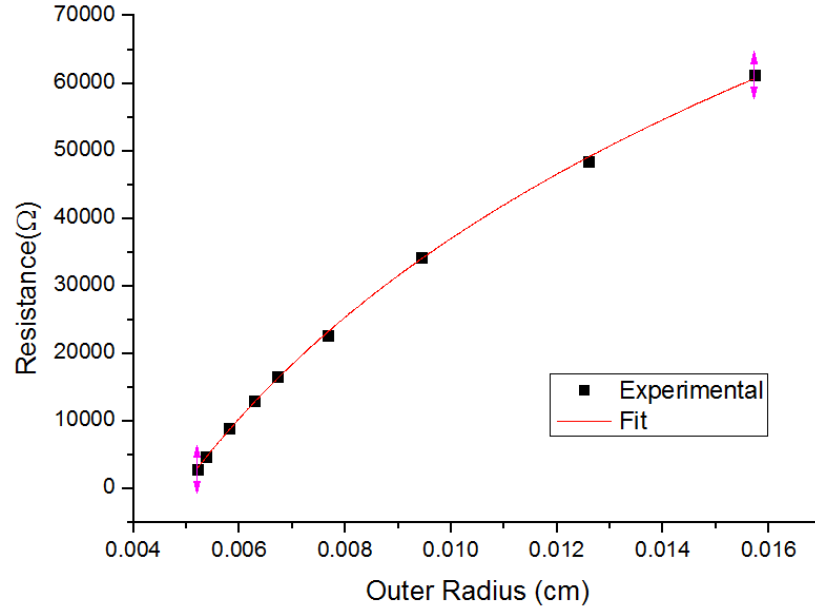


Figure 3.19: Graph of resistance between circular contact pads against outer contact test pad radius.

The two point probe method was employed in measuring the resistance between test contact pads in this work. One probe was placed on the large metal contact pad and the other was placed on the circular test contact pad. Both probes were connected to a source measure unit, Keithley 238, to perform I-V measurements by sourcing a DC voltage changing from -2 V to 2 V in a step of 0.1 V.

3.4. Scanning Electron Microscope

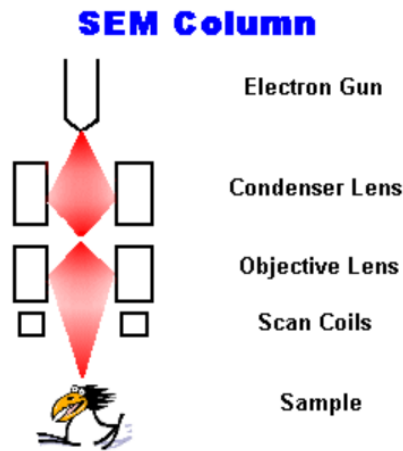


Figure 3.20: The optical column unit inside the scanning electron microscopy [7].

Scanning Electron Microscopy (SEM) is a powerful microscopic tool for inspecting the surface topology of a target material. As its name suggests it utilises a high energy electron beam to interact with the target surface instead of visible light to generate images. A high magnification of 300,000x image can be easily obtained at a high contrast for device fabrication or scientific investigations such as surface topology of a metal contact and cross-sectional structure of wafer bonded substrates. During the operation of obtaining a SEM image, a spray shape of high energy electron is first generated from an electron gun and this spray of electron then goes through a series of charged electrodes that act like condenser lenses and objective lenses to become a focused electron beam as seen in Figure 3.20. When this electron beam scans across the target area intended for investigation, the incident electrons, also known as primary electrons, can interact with the target in three ways: First, It can simply goes through the material without interacting with any atoms inside the target material. Second, it can hit and remove the electrons from the atoms inside the target material [7]. The removed electrons, also known as secondary electrons, are then collected by a positively charged secondary electron detector and then analysed to produce an image [7]. Third, if the primary electrons hit the nuclei of the atoms inside the target material instead of electrons, the primary electrons are scattered back, producing a backscattered electrons. These backscattered electrons can then be collected by a backscattered electron detector and

analysed to produce an image. Thus, SEM images can be produced by using either the secondary electrons or the backscattered electrons. The secondary electron images are very useful when the surface topology of the target material is being investigated. While the backscattered electron images are very useful when differentiating one material from another. This is because the number and energy of the backscattered electrons depend on the type of nuclei from atoms inside the target material. Materials with low atomic weight will generate less backscattered electrons than material with high atomic weight. The processed backscattered electron image is shown as a density plot of backscattered electrons collected from the investigated surface. As a result, the material with low atomic weight appears as a dark spot and the material with higher atomic weight appears as less dark spot, as illustrated in Figure 3.21.

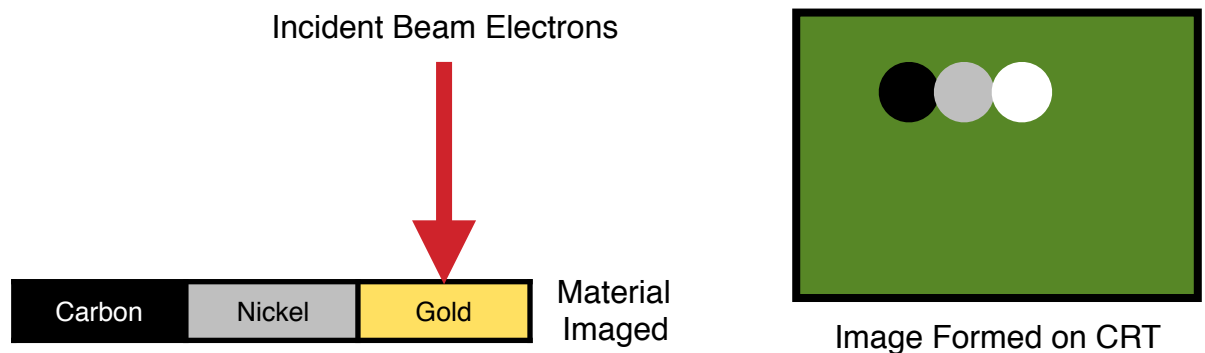


Figure 3.21: The schematics of image processed using backscattered electrons collected from carbon, iron and gold.

3.5.Cross-sectional Photoluminescence and Raman Scattering

When light is applied to a material, the photons can be absorbed, reflected or transmitted through the material or scattered. The interaction with the incident light is strongly dependent on both of the material and the energy of the photons. When the incident light gets scattered, it can be scattered in two ways - inelastic scattering and elastic scattering. In elastic scattering, also known as Rayleigh scattering, the incident photons excite the electrons in the material to a higher virtual energy level from which they relax back to the original energy level as shown in Figure 3.22 In other words, the magnitude of the incident photon does not change and is totally scattered at the same energy level [8]. When the scattered incident photon is inelastic, also known as Raman

scattering, the incident photon excites the electron to a higher virtual energy level and relax back to either a lower energy level (anti-stoke Raman scattering) or a higher energy level (stoke Raman scattering) [9]. In other words, the incident light is either scattered back at a shorter wavelength or longer wavelength.

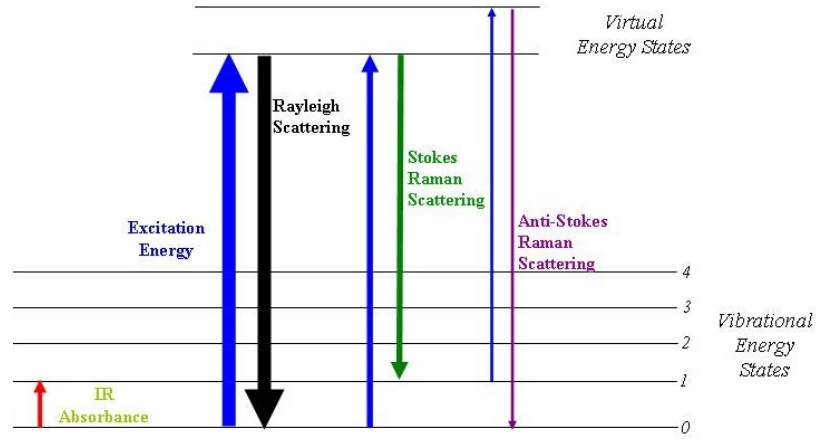


Figure 3.22: Schematics of Rayleigh scattering, stokes Raman scattering and anti-stoke Raman scattering [8].

Raman spectroscopy collects the inelastic scattering of a monochromatic light beam applied to the target material. This applied monochromatic light beam interacts with molecular structures and then scatters back photons with higher or lower energy than the incident light photons. Since molecular structure or chemical bond has a unique vibrational mode, it can give a unique change in the energy of the incident photons and provides a vibrational mode characteristics of the material [9].

These vibrational modes can be affected by the stress, carrier concentration and temperature. Thus, by studying the energy difference between the initial energy level and the final energy level or the Raman shift (ν) as illustrated in equation 3.7 [10], the variations of stress, carrier density and temperature in the material can be measured.

$$\nu = \frac{1}{\lambda_{incident}} - \frac{1}{\lambda_{scattered}} \quad (3.7)$$

Wurtzite GaN has been studied to have eight vibrational modes including two A_1 , two B_1 , two E_1 and two E_2 . The A_1 mode at 734 cm^{-1} and E_1 at 741 cm^{-1} are due to interaction with acoustic phonons. The other A_1 mode, two B_1 , one E_1 and two E_2 modes are optical phonons, which can behave as either transverse optical (TO) or longitudinal optical (LO) modes [10]. The Raman shift of peak wavenumber of those vibrational modes are A_1 (TO) at 532 cm^{-1} , B_1 (low energy) at 337 cm^{-1} , B_1 (high energy) at 720 cm^{-1} , E_1 (TO) at 559 cm^{-1} , E_2 (high energy) at 567 cm^{-1} and E_2 (low energy) at 144 cm^{-1} [11]. However, only A_1 (TO), E_1 (TO) and the two E_2 optical phonon modes are Raman active. The E_2 (high energy) mode is probably the most useful among all other modes. This is because information about the stress and crystal quality can be determined from it. Since the concentration of impurities and point defects in the GaN epitaxy can lower the lifetime of phonon, the line width of the E_2 vibrational mode can reveal the crystal quality of the GaN, an increase in the line width of the Raman peak implies a high concentration of either impurities or point defects within the GaN epitaxy. While the stress status of a GaN layer can be determined by the Raman shift of the peak wavelength of E_2 vibrational mode. In stress-free GaN the E_2 Raman peak appears at 567 cm^{-1} . If there is an increase in the wavenumber of the Raman peak, it indicates that the GaN is under compressive stress, a decrease in its wavenumber indicates that the GaN is under tensile stress [12].

Photoluminescence is a different process from Raman scattering, It involves exciting electron-hole pairs in the target material by exposing it to a laser beam with a higher energy than the band gap energy of the target semiconductor and collects light re-emitted light. The photo-generated electron-hole pairs in the semiconductor material, which recombine and the emitted photons have energy corresponding to the characteristics of the recombination process. Since each material has its unique molecular structure and band gap, studying the remitted light can give information of the material. For instance, the band edge emission of a stress free GaN is at the a wavelength of 367 nm [13]. If there is a red-shift in the PL spectrum with respect to the band edge emission wavelength, the GaN is under tensile stress [13]. A blue shift is a characteristics of compressive stress. Also the full-width half maximum (FWHM) of the band edge photoluminescence provides another measure of the crystal quality of the

epitaxy. Broadening of the FWHM is an indication of decrease in crystal quality, which can be attributed to the presence of high concentrations of point defects, impurities and threading dislocations.

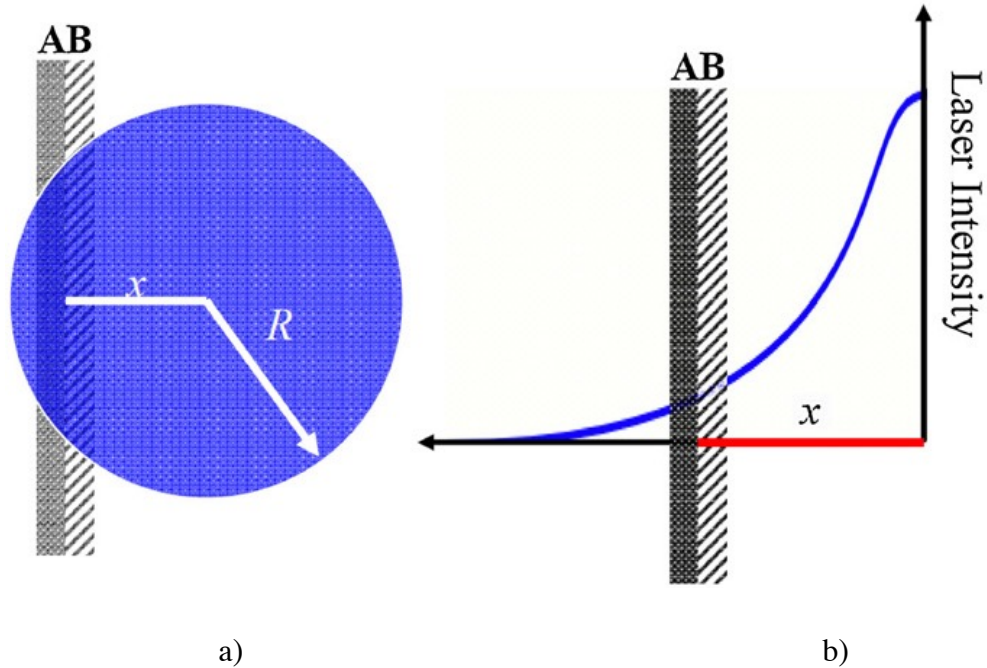


Figure 3.23: Schematic of a) a laser spot aligns on to a dual layer structure and b) laser intensity varying as a Gaussian profile [14].

An LED is made of different layers of GaN based epitaxy materials, these materials have different lattice constants, causing the stress to vary from layer to layer. For instance, it is well-known that an InGaN quantum well grown on a GaN confinement layer is under compressive stress as GaN layer has a smaller lattice constant than that of InGaN. Therefore, it is important to measure the stress layer by layer. This can be done method developed by Jiang et al. [14]. It can be seen from Figure 3.23 that when a circular laser beam with gaussian intensity profile approaches the edge of a GaN structure consisting of layers A and B. GaN layer B will be exposed to a slightly higher laser power due to the rapid intensity variation at the edge of the laser beam and hence give a slightly higher signal PL or Raman signal. Since the radius of the laser spot (R) is much larger than the layer thickness (d), the distance between the centre of the laser spot and the edge of the dual layer structure (x), this relation can be written as $d \ll x < R$. As it can be seen in Figure 3.23b that the Gaussian intensity profile of the laser beam, the laser intensity incident on both layers is still suffering similar that the change in laser power across the layers A and B can be approximated

by a trapezium shape. if the layer thickness are much smaller than the laser beam diameter [14]. Therefore, The PL or Raman signal strength is proportional to the area of trapezium and the signal ratio of layer A to layer B (S_A/S_B) can be given by [14]

$$S_A / S_B \approx \frac{d \times \frac{2 \times \sqrt{R^2 - (x-d)^2} + 2 \times \sqrt{R^2 - x^2}}{2}}{d \times \frac{2 \times \sqrt{R^2 - (x+d)^2} + 2 \times \sqrt{R^2 - x^2}}{2}} \quad (3.8)$$

Since d^2 is much smaller than other terms in equation (3.8), by the latter may be approximated

$$S_A / S_B \approx \frac{1 + \frac{\sqrt{R^2 - x^2 + 2xd}}{\sqrt{R^2 - x^2}}}{1 + \frac{\sqrt{R^2 - x^2 - 2xd}}{\sqrt{R^2 - x^2}}} \quad (3.9)$$

Which on re-arranging becomes

$$\frac{S_B}{S_A} \approx \frac{1 + \sqrt{1 + \frac{2xd}{R^2 - x^2}}}{1 + \sqrt{1 - \frac{2xd}{R^2 - x^2}}} \quad (3.10)$$

Assuming $\frac{2xd}{R^2 - x^2} \ll 1$ and $\left(\frac{2xd}{R^2 - x^2}\right)^2$ is negligible, equation (3.10) yields

$$\frac{S_B}{S_A} \approx 1 + \frac{d}{\frac{R^2}{x} - x} \quad (3.11)$$

It can be seen from equation (3.11) that a large signal ratio (S_A/S_B) can be achieved when the edge of laser spot begins to overlap to the dual layer structure (i.e $x \approx R$).

The exposure of the edge of a dual layer structure to a laser beam of Gaussian beam profile can be represented in another way. The laser intensity, $I(x)$, varies with the beam radius, which is represented by a Gaussian [14]

$$I(x) = ae^{-\frac{r}{b}} \quad (3.12)$$

where a and b are constants. Therefore, the Raman and PL signal strength ratio also can be re-written as [14]

$$\frac{S_B}{S_A} = \frac{1 + e^{\frac{2xd}{b}}}{1 + e^{-\frac{2xd}{b}}} \quad (x \gg d > 0) \quad (3.13)$$

Note, it is possible for the signal ratio (S_A/S_B) to be large when the laser spot is fully exposed to GaN layer B and just partially exposed to layer A [14]. Using these properties, the local variation of stress in the individual layer of GaN based LED wafer can be determined by comparing the PL or Raman spectra measured when the laser beam scans cross-sectionally across a LED wafer.

3.6.References

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Chapter 4

Investigation of Reflective Ohmic Contact to p-GaN

4.1.Introduction

The electrical contact on GaN-based Light Emitting Diodes (LEDs) are usually made of thin multiple layers of metals designed to provide a good electrical interface between the power source and the GaN with ideally no additional electrical resistances or changes to the current to voltage (I-V) performance of epitaxy. However, all kind of contacts must carry electrical resistance, which can have a poor impact on the performance of devices. A poor LED electrical contact with a large resistance can lead to a large voltage drop across the metal to LED epitaxy interface. As a result, the contact resistance should be kept as low as possible, so that the forward biased voltage of the LED is kept to as low as possible to maximize electrical to optical power efficiency. When designing the contacts for LED devices, an ohmic contact is generally preferred as it provides a low contact resistance and a quasi-linear I-V characteristic [1]. Therefore, only a small amount of power is consumed on the contact and the I-V characteristics of devices are not distorted [1].

In a GaN on Si LED, the contact to p-GaN plays an important role. This is because the Si growth substrate can absorb the light, which is emitted by the active region propagating to the direction of Si growth substrate, reducing the light extraction efficiency. To resolve this issue, a reflective p-type contact together with the vertical LED (VLED) structure is used. To realize the VLED structure, the original growth substrate has to be removed and the LED epitaxy is transferred to a carrier substrate with a highly reflective p-type contact, so that the light emitted by the active region is reflected rather than being absorbed by the carrier substrate. Thus, the contact to p-GaN not only has to provide a

low resistant electrical connection between the power source and the p-GaN layer, but also to provide a highly reflective surface as shown in Figure 4.1. However, low resistant p-GaN ohmic contacts are difficult to form. This is because it is difficult to find metals or conducting oxides with work functions larger than that of p-GaN ($\phi_{p-GaN} = 6.5 \text{ eV}$) [1]. Therefore, forming a low resistance p-GaN ohmic contacts by using metals with work function larger than that of p-GaN semiconductor layer is challenging. Furthermore, p-GaN layer is usually doped using Mg, which requires a high activation energy for Mg acceptors ($\sim 170 \text{ meV}$) and the Mg acceptors can form Mg-H complex, which requires 1.5 eV to activate [1]. Thus, it is very difficult to produce p-GaN with carrier concentration higher than $\sim 10^{18} \text{ cm}^{-3}$ and hard to form a thin p-GaN layer with high carrier concentration on the surface of p-GaN layer for holes to tunnel through.

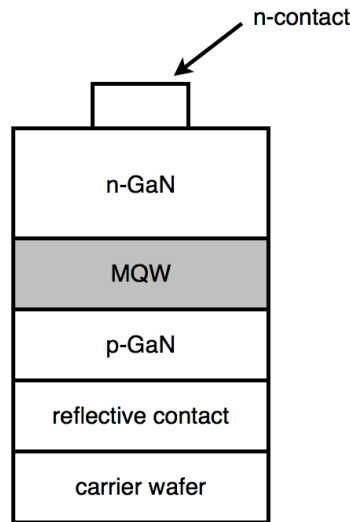


Figure 4.1: A vertical LED structure with a p-type contact as a mirror contact.

The traditional Nickel/Gold (Ni/Au) p-type ohmic contact is widely used and well known to provide low contact resistivity of $1.15 \times 10^{-4} \Omega \text{cm}^2$, but it is nearly transparent (only has reflectivity of 22 %) and not reflective enough as a reflector. Thus, it cannot be used for the GaN on Si VLEDs being developed in this study. Silver (Ag) appears to be a strong candidate to make a good ohmic contact to p-GaN. It is a well known reflective material, which is capable of providing 92 % reflectivity at the wavelength of 460 nm and having a moderate work function ($\phi_m = 4.74 \text{ eV}$). However, it is also well known that it is not thermally stable and agglomerates under high temperature condition [2],

resulting in degradation of its electrical and optical properties. In this work, the electrical and optical properties of Ag based contact to p-GaN is investigated as a function of annealing temperature. It also demonstrates that the Ag agglomeration can be significantly suppressed by inserting thin Ni interlayer, which leads to a significant improvement of contact resistivity and reflectivity.

4.1. Ohmic Contact

An ohmic contact is defined as a metal-semiconductor contact that has a linear or quasi-linear I-V characteristic under forward- or reverse-biased conditions [3]. The typical I-V characteristics of an ohmic contact and schottky contact are illustrated in Figure 4.2.

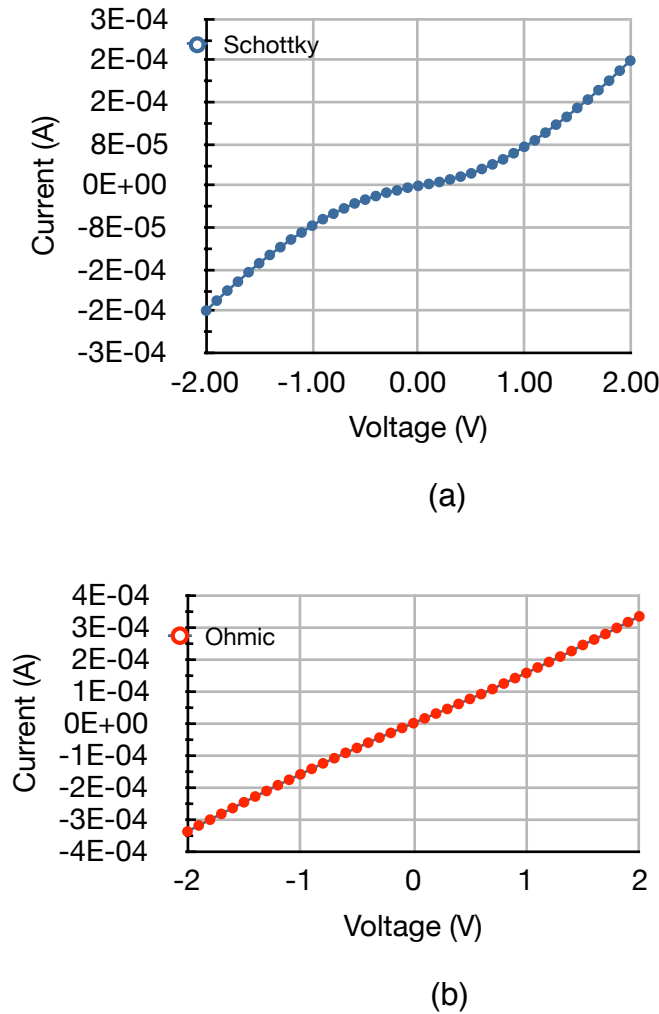


Figure 4.2: Current-voltage characteristics of (a) schottky contact and (b) an ohmic contact.

Under a high current density condition, metal contact self heating can cause the metal atoms to migrate and then diffuse through threading dislocations in the

semiconductor, to eventually short-circuit the junction. Therefore, a good ohmic contact should have low specific contact resistivity and good thermal stability, so that the metal self heating is minimized. In addition, it should only have a negligible voltage drop across the metal-semiconductor interface compared to the LED device, so only small amount of energy is dissipated in the contact.

4.2.Metal Contact On p-type Semiconductor

Forming a good ohmic contact to a semiconductor is not an easy task and the metal deposited to the semiconductor must be carefully designed. When a metal is deposited onto a semiconductor, the carriers will flow across the metal to the semiconductor until the system is in an equilibrium state (i.e. Fermi levels of metal and semiconductor are equal in energy) [3]. Therefore, when a metal contact is in contact with p-type semiconductor, if there is a difference between the metal contact work function ($q\Phi_m$) and semiconductor work function ($q\Phi_s$), the holes near the surface of the semiconductor will diffuse into the metal in order to reach the equilibrium state (N.B work function is defined as the minimum energy required to remove an electron from the material, so it is defined as the energy difference between the vacuum level and Fermi level [2]). As the holes leave the semiconductor, the acceptors near the surface of the semiconductor are left negatively charged and then create positive charges on the surface of metal. These ionized acceptors and positive charges on the surface of metal create a space charge region that repels the flow of holes and acts like a barrier, namely Schottky barrier (Φ_B), at the metal-semiconductor interface. The height of Schottky barrier reflects the mismatch between the work functions of metal and electron affinity of the semiconductor. In this model, the Anderson model of junction formation, the bigger the mismatch between the work functions of metal and affinity of semiconductor, the higher the Schottky barrier. Therefore, the ideal Schottky barrier height when the metal is contact with the p-type semiconductor can be represented by the following equation [4]:

$$q\Phi_B = E_g - q(\Phi_m - \chi) \quad (4.1)$$

Where, Φ_m is work function of the metal, Φ_B is the Schottky barrier height of p-type semiconductor, E_g is the band gap energy of the p-type semiconductor, χ is

the electron affinity of the semiconductor and q is the element charge of an electron.

Figure 4.3 illustrates the Schottky barriers formed at the metal to p- and n-type semiconductor interfaces when the work function of the metal is larger than that of n-type semiconductor and is smaller than that of p-type semiconductor respectively.

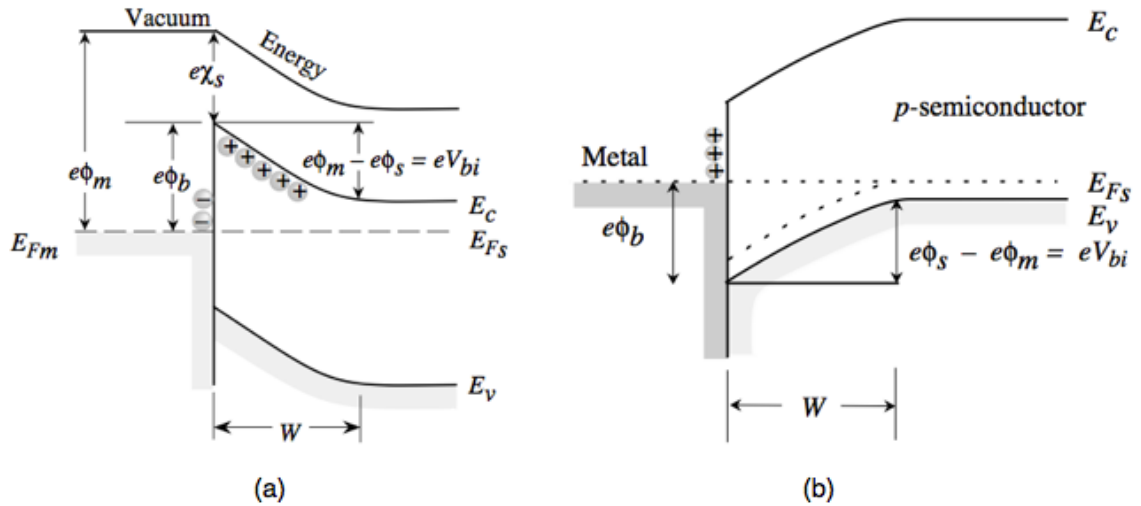


Figure 4.3: (a) Schottky barrier formed by n-type semiconductor and (b) Schottky barrier formed by p-type semiconductor [4].

Since the Schottky barrier height is only dependent on the work functions of the metal and semiconductor electron affinity [4], the barrier height can be easily varied by using only metals with different work functions. In addition, it is intuitively clear that an ohmic contact can be obtained if the Schottky barrier height is reduced. Thus, choosing the metal with an appropriate work function allows the contact to become ohmic. Figure 4.4 illustrates the p-type metal contacts with different work functions on a p-type semiconductor. It can be seen on Figure 4.4(a) that when the work function of metal is smaller than that of the p-type semiconductor, the valence band of the p-type semiconductor bends downwards due to the formation of space charge region (hole depletion region) [5], creating a barrier. For carriers to travel from the metal to the semiconductor, they must overcome the Schottky barrier. This Schottky barrier makes the electrical property of the metal to semiconductor junction rectifying and hence behaving as a high resistance rectifying contact, which does not provide a linear current-voltage characteristic. As illustrated in Figure 4.4(c), when the work

function of metal is larger than that of the p-type semiconductor, the holes from the metal flow to the semiconductor to achieve equilibrium state. This flow of holes creates a hole accumulation region near the surface of semiconductor, which leads to the valence band to bend upwards. The resultant barrier is small or negative. This situation is favourable for obtaining an ohmic contact as the holes in the metal experience the least barrier and are free to flow into the p-type semiconductor.

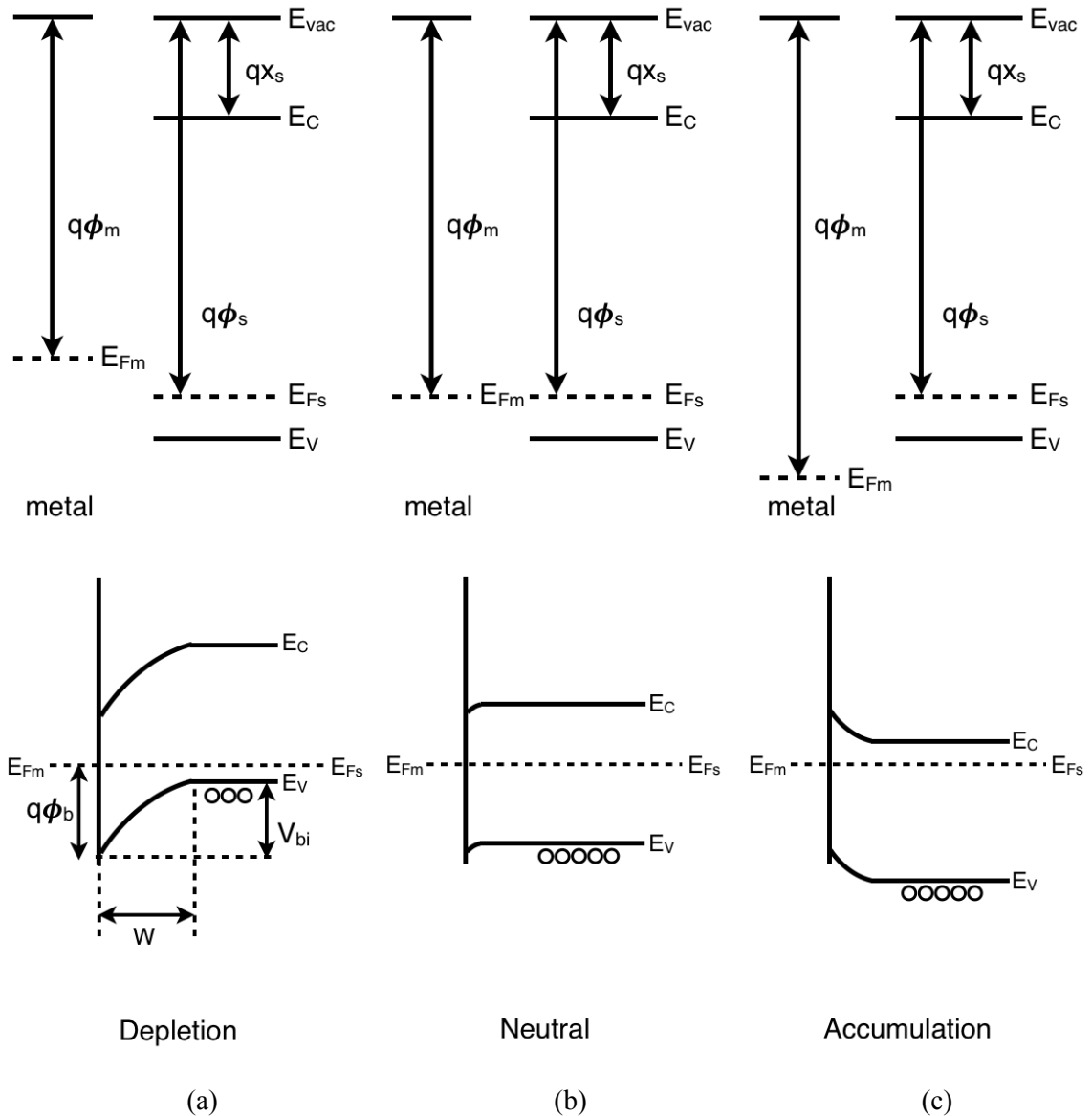


Figure 4.4: The schematics of metal contact to p-type semiconductor (a) $q\Phi_m < q\Phi_s$, (b) $q\Phi_m = q\Phi_s$ and (c) $q\Phi_m > q\Phi_s$.

Figure 4.5 illustrates an LED with a p-type ohmic contact attached to the p-type semiconductor. It can be seen that when the LED is forward biased, holes are injected into the semiconductor. The holes flowing from ohmic the metal to the

semiconductor interface encounter only very small barrier, which is eventually removed if the forward biased voltage reaches the amplitude that the valence band edge is higher than the Fermi level of the metal.

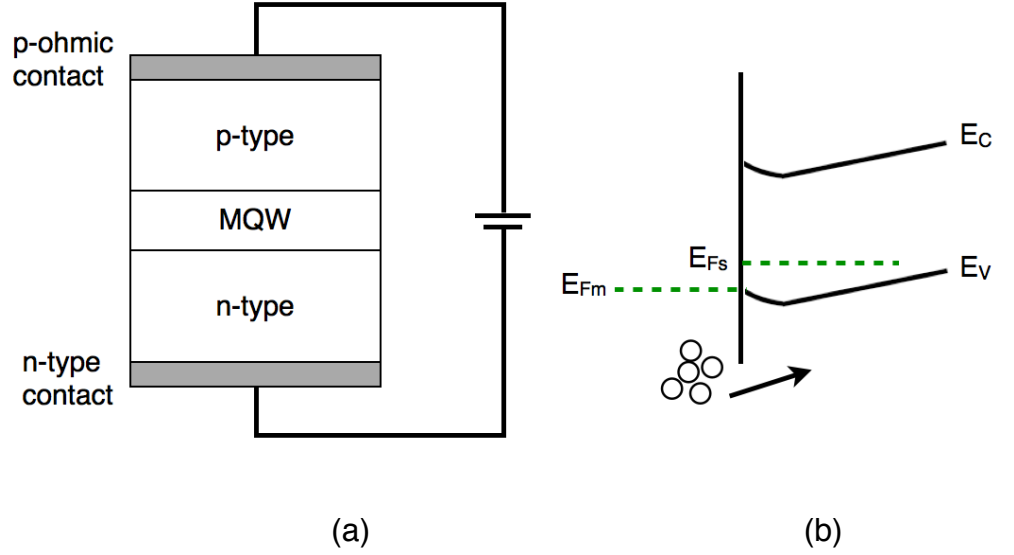


Figure 4.5: The schematics of (a) an LED with p-type ohmic contact and (b) band diagram when p-type ohmic contact under forward biased condition.

Obtaining a p-type ohmic contact by using a metal with a large work function is not the only option. An ohmic p-contact can also be achieved by heavily increasing the acceptor concentration (N_A) of the surface of semiconductor. The width of space charge region (W), $W \propto N_A^{-1/2}$ as illustrated in equation (4.2) [5]. Thus, the width of space charge region of a heavily doped semiconductor is very thin and carriers can readily tunnel through the space charge region to the semiconductor from the metal, forming in effect an ohmic contact. As holes tunneling from the metal contact to the p-type semiconductor can be hard to image, it is helpful to consider as electrons tunneling from the valence band of p-type semiconductor to the metal contact.

$$W = \sqrt{\frac{2(V_{bi} - V_a)\epsilon_s}{qN_A}} \quad (4.2)$$

Where W is width of space charge region, V_{bi} is built-in potential barrier that holes encounter when traveling from the semiconductor to the metal (for the case of p-type semiconductor), V_a is biased voltage, ϵ_s is permittivity of the

semiconductor, N_A is acceptor concentration of the semiconductor, q is the elemental charge of an electron.

Figure 4.6 illustrates the carrier transport mechanisms for p-type semiconductor under lightly and heavily doped conditions ($q\phi_m < q\phi_s$). It can be seen from Figure 4.6(a) that a Schottky barrier is formed at the metal-semiconductor junction due to the work function mismatch between the metal and semiconductor. The holes from the metal can only pass this barrier if they have enough thermal energy (i.e. the holes are thermally excited to pass over the barrier). This current transport mechanism is known as Thermionic Emission (TE) [6]. Considering a lightly doped semiconductor at room temperature, only a small amount of holes have enough thermal energy to travel across the barrier. As the p-type semiconductor is lightly doped causing the width of space charge region to become thick, carriers cannot tunnel through to the p-type semiconductor, the only way that the holes can pass the barrier is via TE.

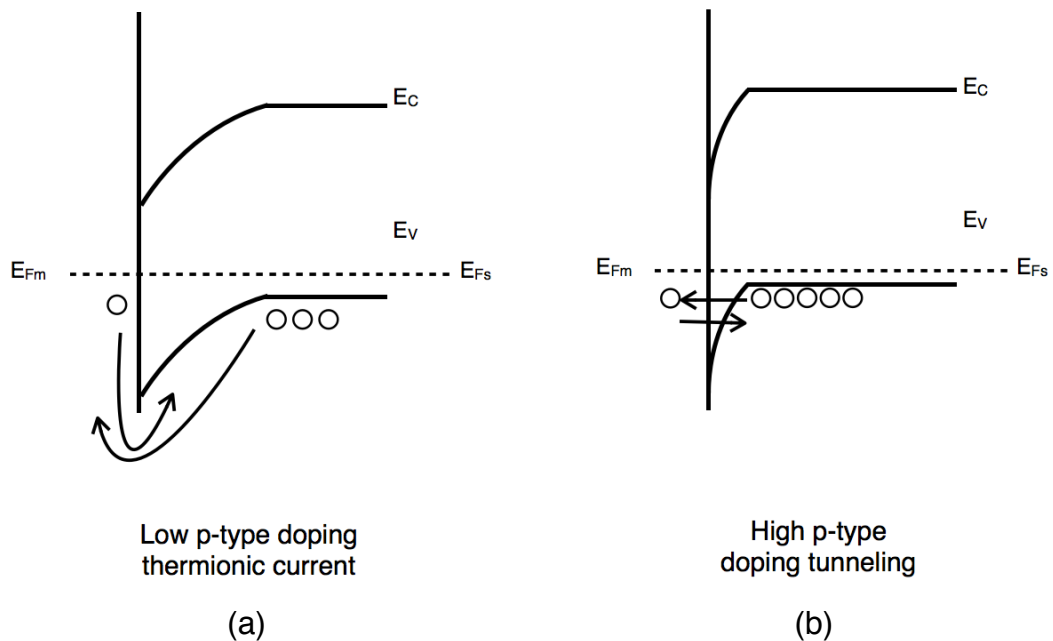


Figure 4.6: Schematics of p-type semiconductor under (a) low doping concentration and (b) high doping concentration.

Figure 4.6(b) illustrates a metal contact deposited onto a heavily doped p-type semiconductor. Tunneling is a quantum-mechanical process in which a hole does not have enough thermal energy to go over the barrier, but they have the probability of penetrating through the barrier to the p-type semiconductor [6].

The tunneling current is proportional to the width of space charge region (W) and can be represented by the following equation [7]:

$$J \propto \exp[-2W \sqrt{\frac{2m_n q(\phi_B - V_a)}{(\hbar/2\pi)^2}}] \quad (4.3)$$

Where W is width of space charge region, m_n is the effective mass of electron, V_a is biased voltage, $q\phi_b$ is Schottky barrier height and q is the elemental charge of an electron.

Thus, the tunneling current transport process significantly depends on the width of the space charge region. The probability of tunneling can be increased by reducing the width of space charge region. Tunneling only dominates the current transport mechanism under a high doping concentration condition or equivalently, when the barrier width is small. This means that by depositing a metal contact on a heavily doped surface of the semiconductor, a metal to p⁺ (+ stands for heavily doped) junction is formed, as illustrated in Figure 4.7, causing the space charge region of metal to p⁺ junction to become thin and hence allows holes to tunnel through the barrier in both directions, resulting a low resistance barrier. Moreover, the resistance of the p⁺ semiconductor to p semiconductor junction is also low. Therefore, the overall resistance between the metal contact and the p semiconductor is low and ohmic.

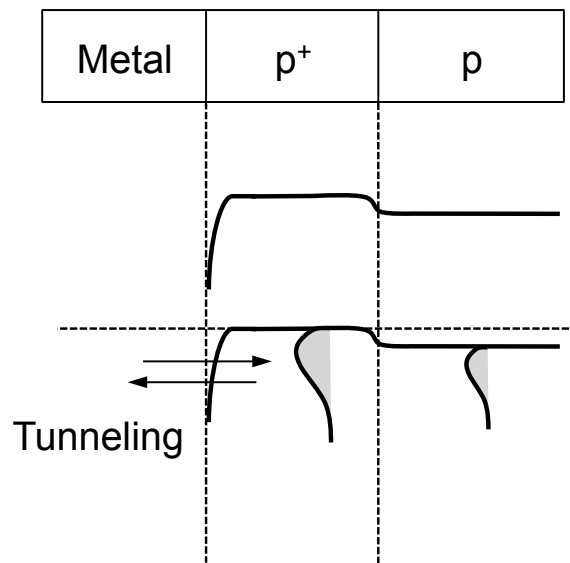


Figure 4.7: Schematic of formation of ohmic contact by using metal-p⁺p semiconductor junction.

4.3. Specific Contact Resistivity

When a metal is evaporated on to a semiconductor, there is a resistance. This resistance are evaluated by two quantities [5]; the contact resistance (R_c), which is dependent on the semiconductor and metal contact used as well as the area of the contact, and the specific contact resistance (ρ_c). Since ρ_c is only dependent on the material of metal contact to semiconductor junction and independent of the area of the contact, it is most often used as a standard quantity to measure the resistance of the metal-semiconductor interface to transfer a current when comparing contacts with different sizes [5]. ρ_c is defined as the interfacial resistance of a unit area between the metal layer and the semiconductor layer [8]. Therefore, this quantity is the summation of several sources, including the metal-semiconductor contact interfacial resistance, part of the resistance of the metal immediately above the metal-semiconductor interface and part of the resistance of the semiconductor immediately below the interface [8]. It can be represented by the following equation [7]:

$$\rho_c = \left[\frac{\partial J}{\partial V} \right]_{v=0}^{-1} \Omega cm^2 \quad (4.4)$$

Where J is the current density flowing through the metal to semiconductor interface, V is voltage drop across the metal to semiconductor interface.

The R_c for contact area A with a uniform current density can be represented by the following equation:

$$R_c = \frac{\rho_c}{A} \quad (4.5)$$

When a metal contact is deposited on a lightly doped semiconductor, and the current transport mechanism is dominated by thermionic emission. The carriers are thermally excited over the barrier as described in the previous section. The current density through the metal to semiconductor due to thermionic emission is given by [7]:

$$J_{th} = A^* T^2 \exp\left(\frac{-q\theta_B}{kT}\right) \left(\exp\left(\frac{qV}{kT}\right) - 1 \right) \quad (4.6)$$

Where A^* is the Richardson's constant $= 4\pi qk^2 m^*/h^3 = 120(m^*/m)$, T is absolute temperature, K is Boltzmann constant, Φ_B is Schottky barrier height, V is biased voltage, m is free electron mass, m^* is effective electron mass

By using equation (4.6) with equation (4.4), one can find the specific contact resistivity for thermionic emission, which is illustrated below [8]:

$$\rho_c = \frac{k}{qA^*T} \exp\left(\frac{q\theta_B}{kT}\right) \Omega \text{cm}^2 \quad (4.7)$$

Therefore, one can conclude from equation (4.7) that the specific contact resistivity is only low if the barrier height is low.

However, when a semiconductor is under heavily doped condition, the width of the space charge region becomes very thin, which allows the carriers to tunnel through. It can be seen from equation (4.8) [7] that the tunneling current is significantly dependent on the space charge region width and increases under high doping condition. Thus, when the semiconductor is heavily doped, tunneling current dominates the current transport, so that the current density will be give by

$$J \propto \exp\left[-2W \sqrt{\frac{2m_h q \theta_B}{(\hbar/2\pi)^2}}\right] \quad (4.8)$$

It is mentioned in the above section that a p-type ohmic contact can be achieved by depositing a metal contact on a heavily doped surface of the semiconductor, which then forms a metal to p+p junction. The space charge region of metal to p+ junction is thin and hence allows the holes to tunnel through the barrier in both ways, resulting low resistance barrier. Moreover, the resistance of the p+ semiconductor to p semiconductor junction is also low. Therefore, the overall resistance between the metal contact and the p semiconductor is low and ohmic. The specific contact resistivity for p-type heavily doped semiconductors, when the current transport mechanism is dominated by tunneling, can be found by using equation (4.8) with equation (4.4), and is shown below [8]:

$$\rho_c \sim \exp\left(\frac{4\theta_B}{h/2\pi} \sqrt{\frac{m_h \epsilon_s}{Na}}\right) \quad (4.9)$$

Where Φ_B is Schottky barrier height, h is Plank's constant, m_h is the effective mass of holes, ϵ_s is dielectric constant of the semiconductor, N_a is acceptor concentration of the semiconductor.

It can be seen from equation (4.9) that the specific contact resistivity for heavily doped semiconductors mainly depends on the acceptor doping concentration and it varies exponentially with $\Phi_B/(N_a^{-1/2})$. Thus, a low specific contact resistivity can be achieved if the doping concentration is high.

4.4. Agglomeration

The contacts of LED devices are often made of several layers of thin metal films, which are generally deposited at low temperature with microstructures not in equilibrium [8]. As a result, these metal films are not thermally stable and their microstructure can change during fabrication processes carrying out in a high temperature environment. These micro-structural changes can cause the instability of the surface morphology of the film, for instance, the formation of small voids or holes in the film surface. These holes in the surface can eventually connect with each other forming isolated islands. Thin films with high surface to volume ratios and weak adhesion to the underlying semiconductor, are easily degraded through such surface morphology changes. The process of a continuous film reducing its surface area to expose the substrate is called agglomeration [9]. An example of an agglomerated metal film is shown in Figure 4.8.

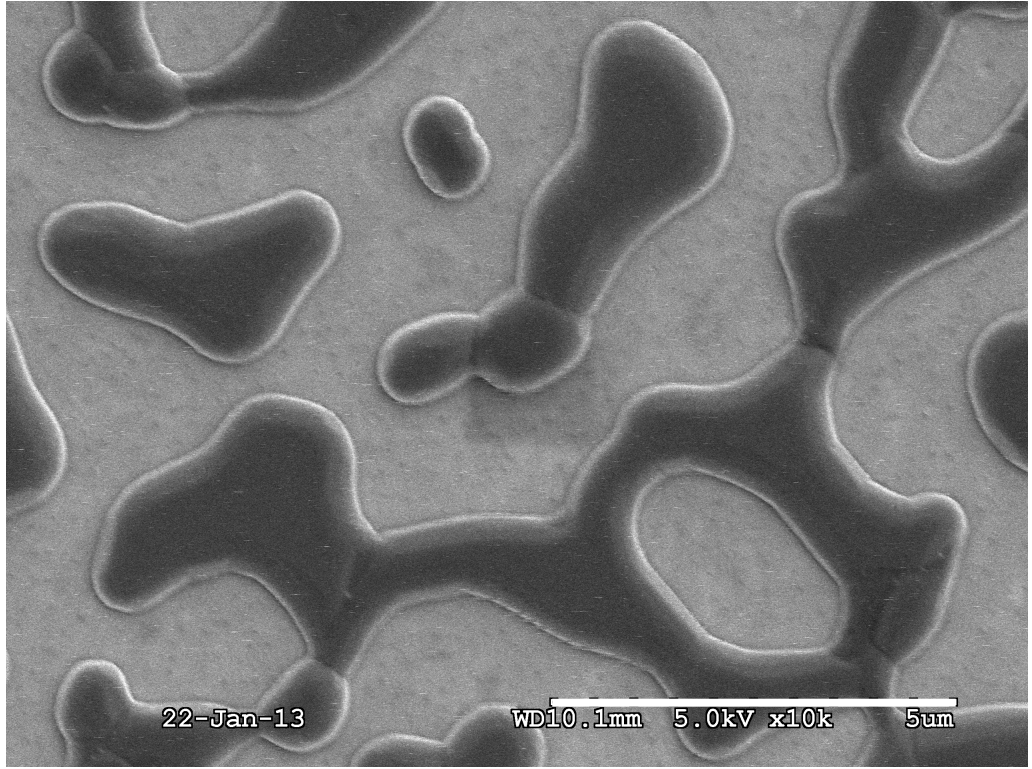


Figure 4.8: Illustration of agglomeration of an Ag thin film.

The system energy can be represented by the following equation [9]:

$$E = A_s\gamma_s + A_g\gamma_g + A_i\gamma_i + A_{sub}\gamma_{sub} \quad (4.10)$$

Where A_s , A_g , A_{sub} and A_i are the areas of metal film surface, grain boundary, substrate and interface between metal film and the substrate respectively. The γ_s , γ_g , γ_{sub} and γ_i are the surface energies of the metal film, grain boundary, substrate and the interface between substrate and the metal film.

The surface energy is defined as the work required to increase the surface area of a material per unit area [10]. Agglomeration is a thermally activated process, which reduces the metal film to substrate system free energy at high temperature. The system free energy can be decreased by reducing the surface area of the metal film and metal film to substrate interface area through atom surface diffusion [11]. Thus, the agglomeration can be triggered by reducing system free energy through decreasing the metal film area and metal film to substrate interface area. Agglomeration usually starts with grain boundary grooving, hillock and hole formation and eventually leading to agglomeration [11]. Grain boundary grooving, which is the phenomenon of the film surface

forming a depression along the intersection of a boundary between two or three grains [11] as illustrated in Figure 4.9. It originates from surface diffusion of metal film atoms where this atom surface diffusion is caused by the thermal stress due to high temperature environment such as annealing.

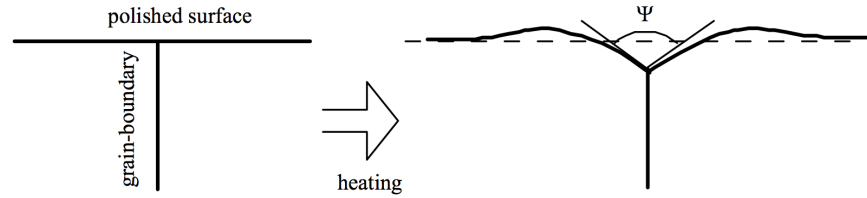


Figure 4.9: The Schematics of grain boundary grooving [12].

4.5.Experimental Details

A 6 inch diameter InGaN/GaN grown on Si LED wafer by metallorganic chemical vapour deposition (MOCVD), was obtained from a commercial source. This wafer has a 650 nm AlGaIn buffer layer with composition of 1470 nm n-GaN, 200 nm thick of InGaN/GaN multiple quantum wells (MQWs) and 95 nm of p-GaN. To examine the p-type specific contact resistivity (ρ_c), the circular transmission line model (CTLM) test structure pattern and a p-type contact pattern were defined on the p-GaN using photolithography for a subsequent lift-off. The contact layers of Ag (200 nm), Ni/Ag (1 nm/200 nm), Ni/Ag (5 nm/200 nm) and Ni/Ag/Ni (1 nm/200 nm/10 nm), which are also tabulated in Table 4.1, were then deposited by using an E-beam evaporator (EBE) and followed by a rapid thermal annealing (RTA) treatment at a temperature range of 300 °C to 500 °C in a step of 50 °C for 2 minutes for subsequent contact resistivity examinations. To test the contact reflectivity the above mentioned contacts were deposited on glass slides for reflectance measurements using a spectrometer.

To measure the contact resistivity of these contacts, the I-V characteristics of the CTLM on p-GaN was measured before wafer bonding process. Whereas, to test light output and I-V performance of these contacts, n-GaN side up LEDs with vertical structure were fabricated using the procedures discussed in section 3.3. The current-voltage (I-V) characteristics was measured using a

Keithley 238. The light output of the Si-VLEDs was examined using an integrating sphere instrument.

| Metallization scheme | Thickness (nm) |
|----------------------|----------------|
| Ni/Ag | 1/200 |
| Ni/Ag | 5/200 |
| Ag | 200 |
| Ni/Au | 5/5 |
| Ni/Ag/Ni | 1/200/10 |

Table 4.1: Metal contact thickness for LED and p-GaN samples.

4.6.Motivation of Ag Based p-type Ohmic Contact

As mentioned in section 4.2, a good quality low resistance ohmic contact can be obtained by having low Schottky barrier or a very thin heavily doped semiconductor layer at the metal interface. A low Schottky barrier can generally be obtained by using a metal with work function close to or larger than that of p-GaN. However, a low resistant p-GaN ohmic contact is generally a lot more difficult to form. This is because, firstly, it is difficult to find metals or conducting oxides with larger/close work functions than that of p-GaN ($\Phi_{\text{p-GaN}} = 6.5 \text{ eV}$) [13]. Secondly, p-GaN layer is usually doped using Mg, which requires a high activation energy ($\sim 170 \text{ meV}$), making it difficult to produce p-GaN with carrier concentration higher than $\sim 10^{18} \text{ cm}^{-3}$ [13]. As a consequence, forming a thin p-GaN layer with high carrier concentration for holes to tunnel through is not practical. Thirdly, since the emitted light of a VLED device is designed to be extracted from the top of n-GaN side, the light that propagates towards the p-GaN side is required to be reflected by the p-type contact. Therefore, designing the p-type ohmic contact for a VLED device is much more difficult as the contact not only needs to be low resistant and ohmic, but also requires highly reflective.

Ni/Au (5 nm/5 nm) has been widely reported to make a good ohmic contact to p-GaN ($\sim 10^{-4} \Omega\text{cm}^2$) by using a thermal treatment in oxygen environment and is considered to be the conventional p-type contact for lateral contact LEDs

[14-16]. However, the Ni/Au contact cannot be used as a reflective contact. This is because it is almost transparent. Its reflectivity after being annealed at 500 °C for 5 minutes is very low (approximately 20 % at the wavelength of 460 nm). Therefore, the conventional Ni/Au contact cannot be used for the VLED devices.

In the absence of metals with work functions larger than p-GaN leaves no choice but to use metals with a work function close to that of p-GaN. Table 4.2 shows three metals with work functions close to p-GaN, namely Gold (Au), Aluminium (Al) and Silver (Ag).

| Material | Reflectance at 460nm wavelength (%) | Work function (eV) |
|----------|-------------------------------------|--------------------|
| Au | 35.7 | 5.1 |
| Al | 92.3 | 4.28 |
| Ag | 92.5 | 4.73 |

Table 4.2: Metals with work functions close to p-GaN ($\Phi_{\text{p-GaN}} = 6.5 \text{ eV}$ [13]).

Figure 4.10 illustrates the reflectance of Ag, Au and Al as a function of wavelength. Although Au has the largest work function of the three metals tabulated in Table 4.2, its reflectivity is very low, which cannot form a reflective contact. Al has a reflectivity at the wavelength of 460 nm approaching 100 %, but its work function ($\Phi_{\text{m}} = 4.28 \text{ eV}$) is rather low. Ag appears to be the best candidate among all three metals as it has a reflectivity at the wavelength of 460 nm close to 100 %, a reasonably large work function and can be easily deposited using by electron beam evaporation.

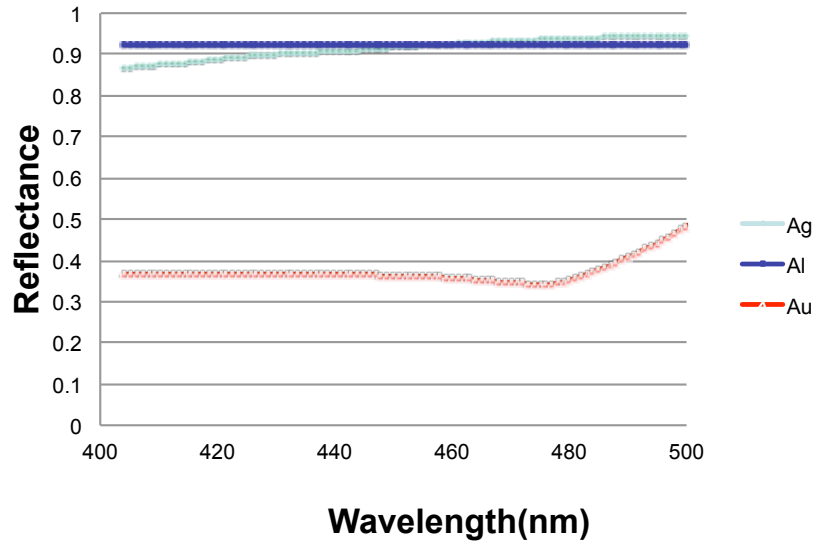


Figure 4.10: The reflectance of Ag, Al and Au as a function of wavelength.

In this work, Ag based contacts on p-GaN are investigated to optimize the metallization scheme as well as the annealing temperature and environment. The specific contact resistivity of Ag based p-type contact was measured by using CTLM test structures. The I-V characteristic, reflectivity and light output of the VLED with Ag based contact were also measured.

4.7. Results and Discussions

4.7.1. Ni/Au contact to p-GaN

It has been widely accepted that Ni/Au forms a good ohmic contact to p-GaN after annealing in oxygen environment for 5 minutes. Therefore, Ni/Au (5 nm/5 nm) were chosen as the benchmark for this work. Ni/Au CTLM test structures were deposited on to the p-GaN sample. The resistances of the nine pairs of test contact pads were calculated from the measured I-V between each set of test contact pads using a Keithley 238 voltage/current source unit and plotted as a function of the outer contact pad radius. The plotted data was then fitted to equation (3.6) to extract the specific contact resistivity. The sample preparation and measurement procedures are detailed in the sample preparation section. According to Ho et al [15], the best Ni/Au contact resistivity can be achieved when Ni and Au are having the same thickness and annealed it at 500 °C in oxygen environment for 5 minutes. Figure 4.11 illustrates the I-V characteristic

of as-deposited Ni/Au(5 nm /5 nm thickness) contacts and after annealing at 500 °C for 5 minutes in oxygen.

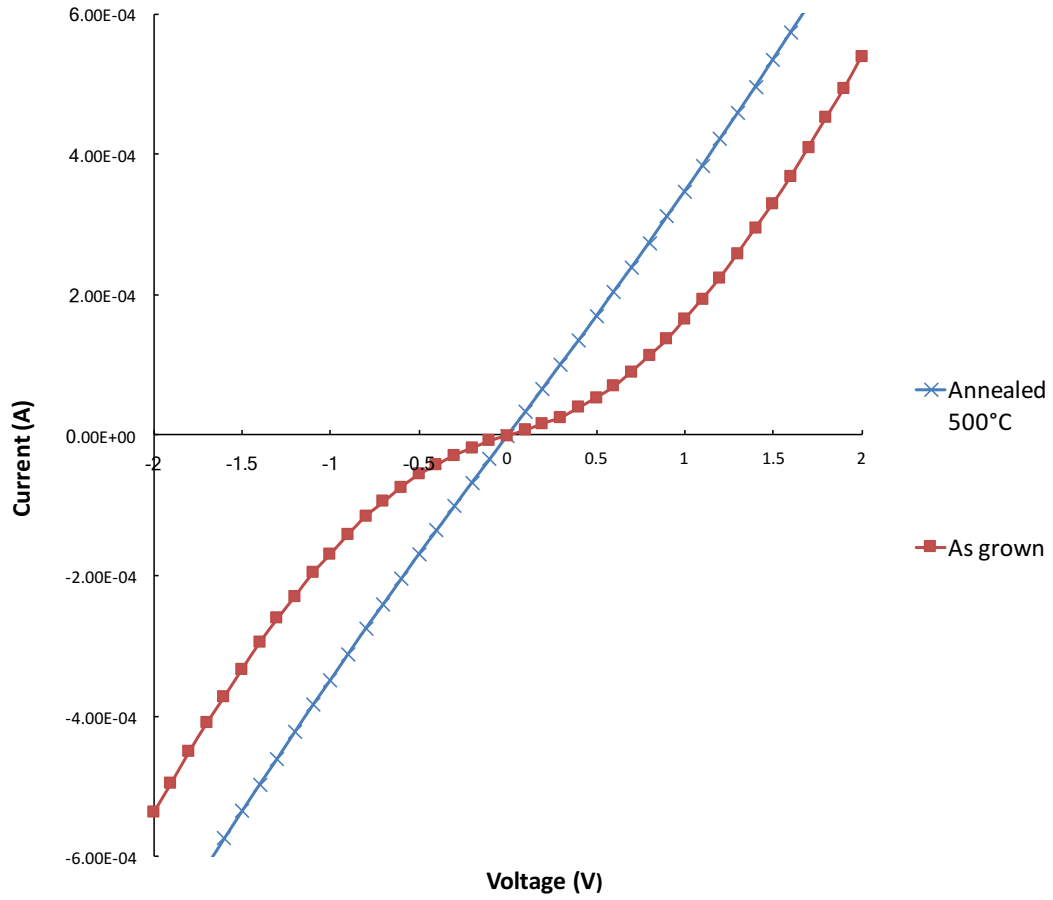


Figure 4.11: The I-V characteristic of Ni/Au (5 nm/5 nm) contact on p-GaN sample before and after thermal annealing, measured from test contact pads spacing of 3 μm .

The I-V characteristic of as-deposited Ni/Au contact has a poor I-V and is clearly not linear. This is due to the large Schottky barrier formed at the contact to p-GaN interface. However, after annealing the Ni/Au in oxygen which causes a noticeable improvement, it shows a linear behaviour and the contact is clearly more conducting. According to Ho et al that the ohmic behaviour of the annealed Ni/Au contact in oxygen can be attributed to the formation of thin NiO interlayer. When the contact is annealed in oxygen, the Ni is oxidized and turned into NiO, while the Au is still remained in metallic form. NiO has a work function of 4.9 eV and can act as a p-type semiconductor [16]. Since Au has a larger work function ($\Phi_m = 5.1$ eV) than NiO, a linear, low resistance ohmic contact is formed at the Au/p-NiO interface. The p-GaN layer forms a p-p

heterojunction with the p-NiO. As a result, an Au/p-NiO/p-GaN junction is formed. Figure 4.12 illustrates the schematic of energy band diagram of this junction under equilibrium condition. Since the work function of the p-GaN is larger than that of p-NiO, the holes in the p-GaN will flow towards the p-NiO resulting an accumulation region formed in the p-NiO layer and an depletion region formed in the p-GaN layer (i.e. the valence band of the NiO bends upwards and the p-GaN valence band bends downwards). Therefore, there are a high density of holes localized in the notch near the p-NiO to p-GaN interface. These accumulated holes can easily get to the p-GaN through thermionic-field emission under forward biased condition when the forward voltage reaches a magnitude that the p-GaN valence band is higher than the Fermi level of p-NiO [15]. The holes flowing from the Au to p-NiO experience very little resistance as Au to p-NiO forms an ohmic contact. Therefore, the overall resistance of Au/p-NiO/p-GaN junction is low.

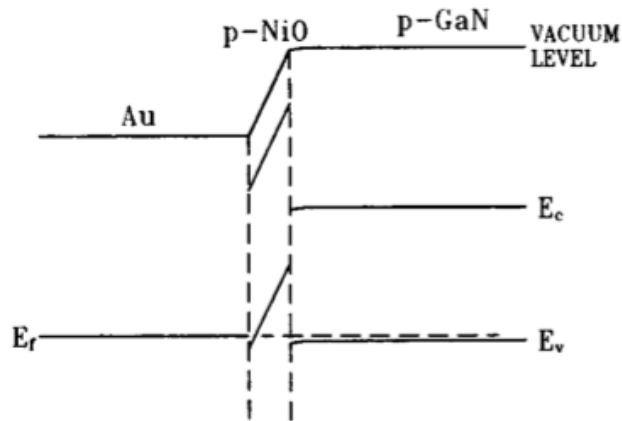


Figure 4.12: Schematics of energy band diagram of Au/p-NiO/p-GaN in equilibrium [15].

To obtain the specific contact resistivity, the resistance between each set of contact pads was measured and plotted against the outer contact pad radius. Equation (3.6) was then used to fit these experimental data points to extract the specific contact resistivity. Figure 4.13 shows the resistance data fitted to the equation (3.6).

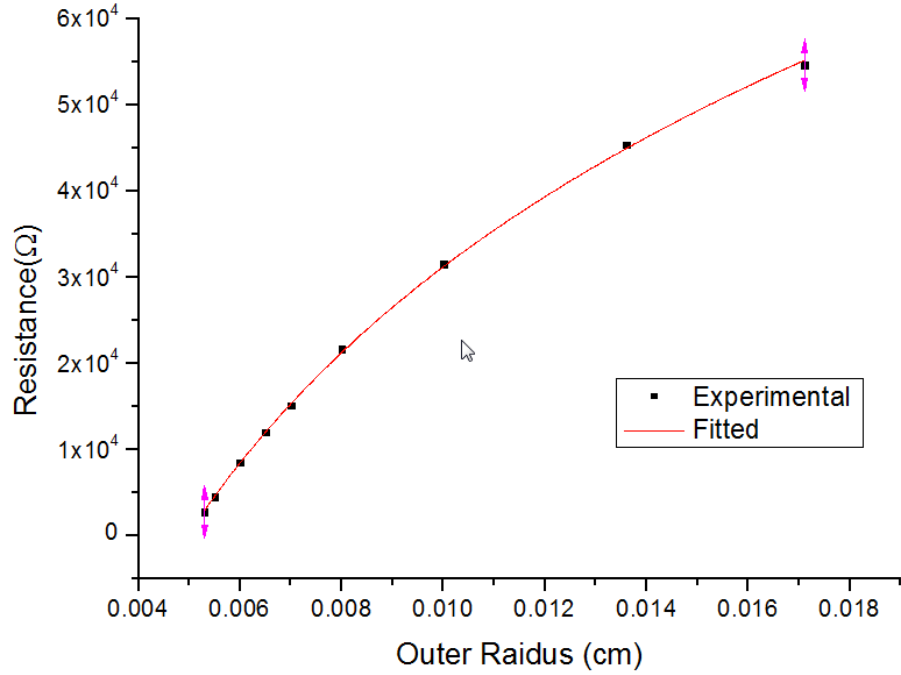


Figure 4.13: Resistance between inner and outer contact pads as a function of separation distance.

The specific contact resistivity of the Ni/Au contact annealed at 500 °C in oxygen environment for 5 minutes was calculated to be $1.15 \times 10^{-4} \Omega \text{cm}^2$, which is low and in agreement with the values obtained by other groups [14-16].

4.7.2. Ag based Contact to p-GaN

After depositing 200 nm Ag on to the p-GaN samples, the I-V characteristic between the outer and inner contact pads on nine pair of the CTLM test structure was measured. A Keithley 238, source measure unit to perform I-V measurements by sourcing a voltage changing from -2 V to 2 V in a step of 0.1 V. Figure 4.14 illustrates the I-V characteristic of the Ag (200 nm) contact without any thermal treatments. It clearly shows that the as-deposited Ag contact to p-GaN does not form an ohmic contact. This poor I-V can be attributed to the large Schottky barrier formed at the Ag to p-GaN interface, found to be $q\phi_b = 2.77 \text{ eV}$, by using equation (4.1).

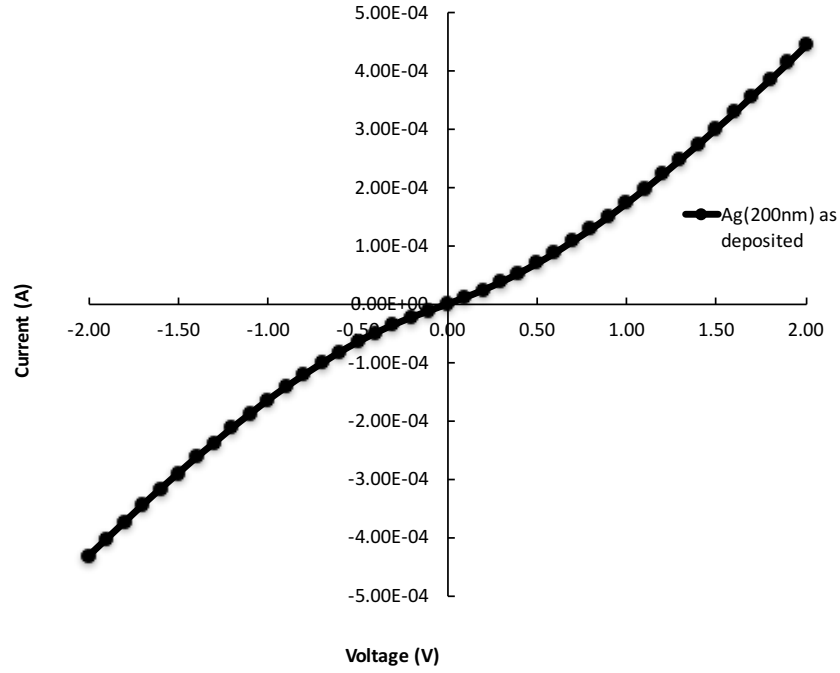


Figure 4.14: The I-V characteristic of as-deposited Ag contact.

Since the as-deposited Ag contact does not form an ohmic contact to p-GaN, a thermal treatment is needed. In order to determine the best annealing environment, the samples were annealed in N_2 and O_2 for 2 minutes at 350 °C. 2 minutes annealing time was chosen as it is known to give the best contact resistivity [17]. Figure 4.15 clearly shows that the thermal treatments in O_2 can noticeably improve the I-V characteristic of the Ag contact. Whereas, the I-V for the Ag contact annealed in N_2 was not linear and less conducting after the thermal treatment. Annealing the Ag contact in O_2 environment appeared to have the best I-V characteristic as it clearly showed a linear behaviour and was conducting the largest current amongst all three I-V. Thus, the annealing environment plays an important role in determining the I-V characteristic linearity and also suggests that annealing the metal contact deposited on p-GaN in oxygen environment is the key to make a good ohmic contact to p-GaN.

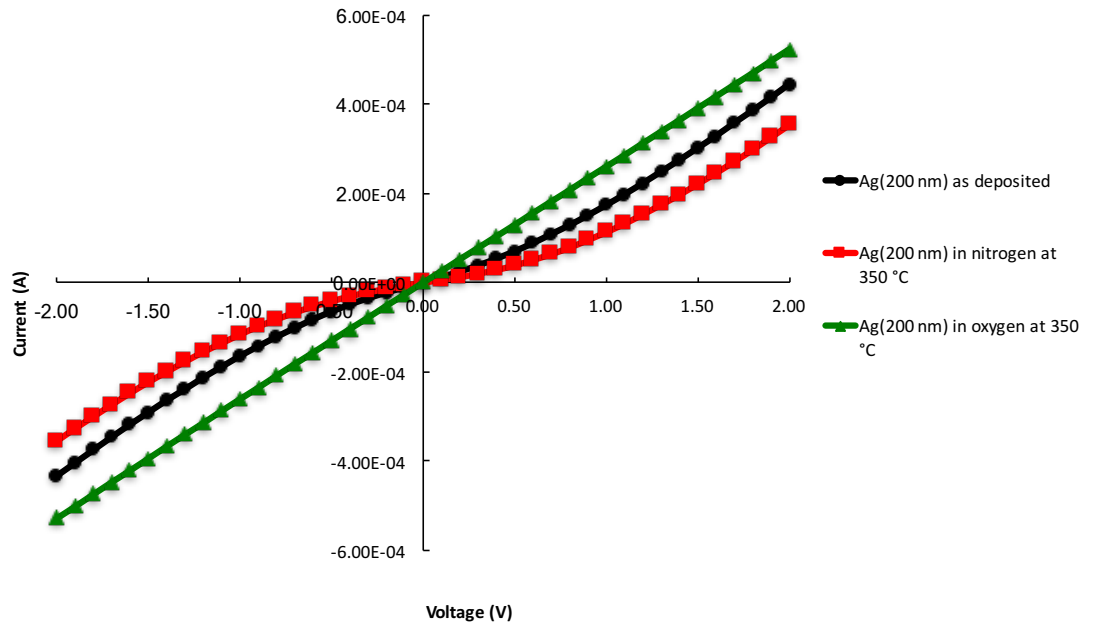
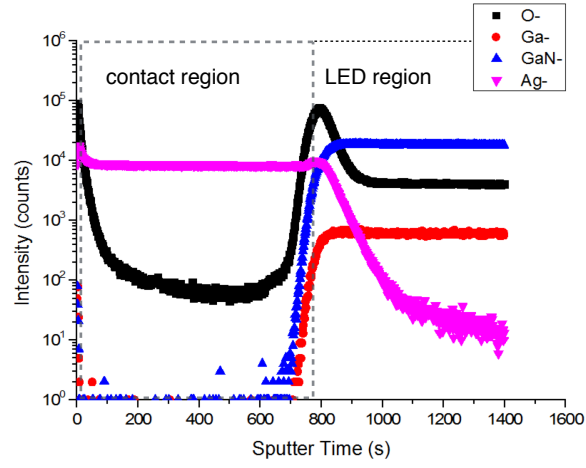
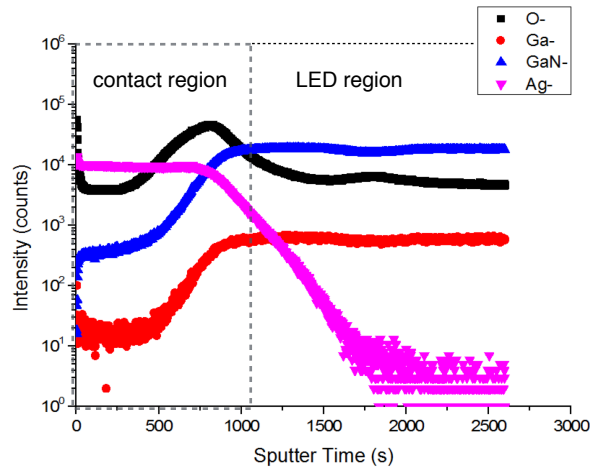


Figure 4.15: The I-V characteristics of Ag (200 nm) contact to p-GaN for as deposited, annealed in N_2 at 350 °C for 2 minutes and annealed in O_2 at 350 °C for 2 minutes.

Figure 4.16 shows the secondary ion mass spectrometry (SIMS) profile of the as-deposited and 2 minute oxygen annealed Ag contacts. It can be seen that the Ag, Ga and N profiles were well defined before the thermal treatment. However, the Ga profile significantly out-diffused into the Ag profile after annealing in oxygen. This suggests that annealing the contact in O_2 causes Ga atoms near the p-GaN surface to out-diffuse into the Ag film due to the high reactivity of oxygen with Ga [18]. The out-diffused Ga atoms then form Ag-Ga solid solution. When Ga atoms out-diffuse, it simultaneously creates Ga vacancies near the p-GaN surface below the contact. It is known that Ga vacancies act as acceptors leading to an increase in hole concentration near the p-GaN surface [18]. As a result, the space charge region width is reduced, which increases the probability of tunneling occurring lead to the formation of ohmic contact. Therefore, annealing the Ag contact in oxygen environment is a critical factor of getting a good ohmic contact to p-GaN.



(a)



(b)

Figure 4.16: The SIMS profile of (a) the as-deposited 200 nm Ag contact to p-GaN and (b) after 2 minute oxygen annealing 200 nm Ag contact to p-GaN.

Figure 4.17 illustrates the sheet resistivity of p-GaN to Ag contact extracted from CTLM test structures. The results show that the sheet resistivity of the p-GaN decreased with increasing the annealing temperature in oxygen environment. The reduction of sheet resistance indicates that the ohmic behaviour of the I-V characteristics after the thermal treatment in oxygen could be attributed to the increase in hole concentration near the Ag to p-GaN interface due to Ga vacancies.

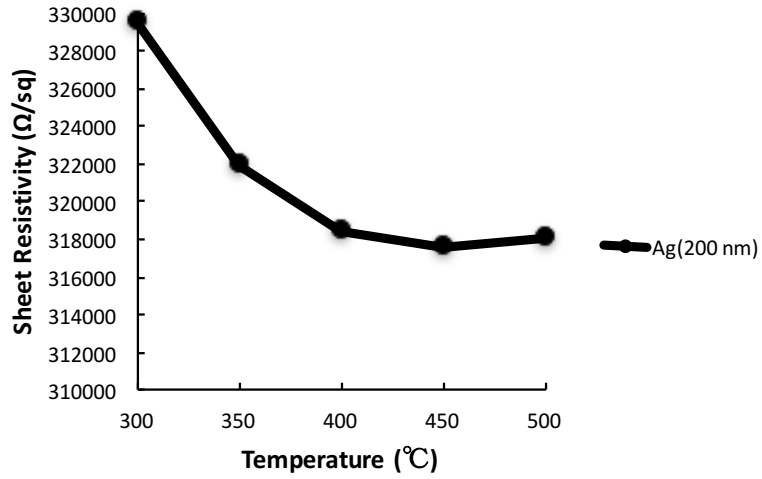


Figure 4.17: The sheet resistivity of p-GaN to Ag contact annealed in 2 minutes under oxygen environment.

To determine the best annealing duration, the CTLM I-V characteristics of Ag-only contact annealed in 2 minutes and 10 minutes in oxygen environment at 350 °C was measured and shown in Figure 4.18. The I-V characteristics of Ag contact after 10 minute annealing in oxygen degraded significantly. It was only conducting 0.075 mA at 2 V after 10 minute annealing compared to 0.52 mA after the 2 minutes annealing contact. The specific contact resistivity was extracted to be $1.5 \times 10^{-3} \Omega \text{cm}^2$ for the contact annealed in 2 minutes and $2 \times 10^{-1} \Omega \text{cm}^2$ for the contact annealed in 10 minutes. Therefore, annealing the contact for 10 minute annealing is too long and 2 minute annealing is more suitable.

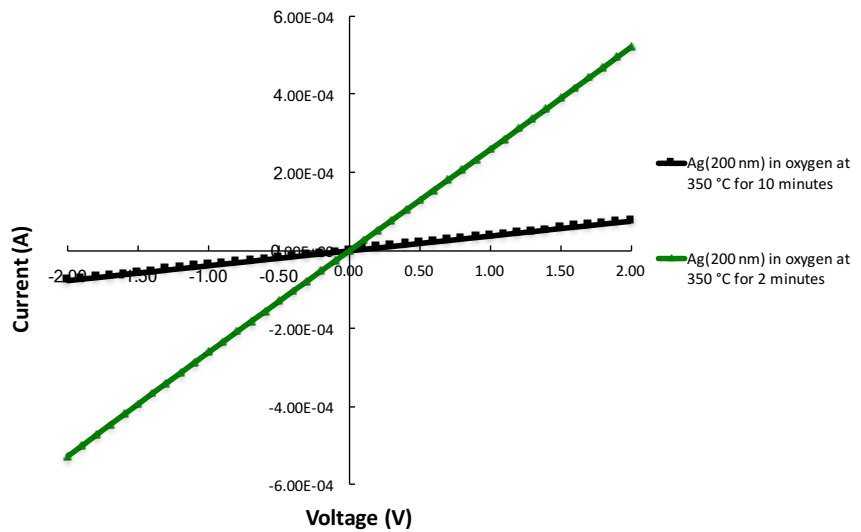


Figure 4.18: Specific contact resistivity of Ag (200 nm) contacts annealed in O₂ for 2 minutes and 10 minutes.

Since 2 minutes appeared to give a better CTLM contact resistivity test, to identify the best annealing temperature, the dependence of temperature test of Ag-only contact was annealed in 2 minutes. Figure 4.19 illustrates the specific contact resistivity of Ag-only contact as a function of annealing temperature for 2 minutes in oxygen. The contact showed a clear reduction trend in the contact resistivity from the annealing temperature of 300 °C to 350 °C and contact resistivity as low as $1.5 \times 10^{-3} \Omega\text{cm}^2$ was achieved at 350 °C. This can be attributed to the increase in the hole concentration near the p-GaN surface. However, as the annealing temperature increased above 350 °C, the contact resistivity started to degrade.

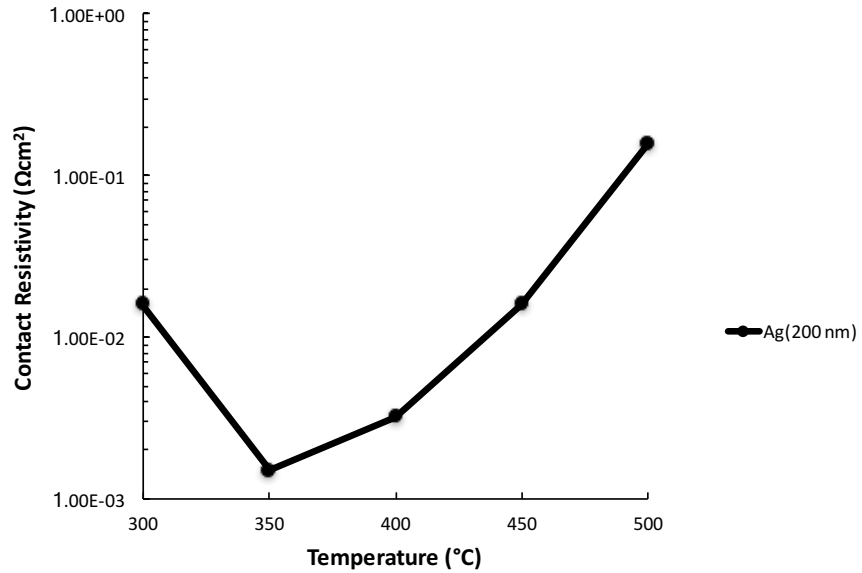


Figure 4.19: The specific contact resistivity of Ag (200 nm) contacts annealed in O_2 for 2 minutes at the annealing temperature range of 300 °C to 500 °C.

The possible cause of the increase in contact resistivity was investigated by examining the surface morphologies of Ag contact surface annealed in oxygen of various temperature for 2 minutes by using Scanning Electron Microscopy (SEM). The results are shown in Figure 4.20. Although the Ag contact after annealing at 350 °C shows an irregular hillock surface with small voids due to agglomeration as illustrated in Figure 4.20(b), the specific contact resistivity was still low. This is because there were only a small number of voids on the Ag contact surface and most of the Ag metal is still in contact with the p-GaN. In addition, the beneficial effect of Ga vacancies in the p-GaN increases the hole

concentration, which could compensate the negative factor of small void formation. However, as the annealing temperature increased, the density and size of the voids also increased. These voids eventually lead to the formation of holes on the contact surface as illustrated in Figure 4.20(d). This hole formation appears to start after 400 °C. As a result, the surface area of Ag metal, which was in contact with p-GaN, was significantly reduced, leading to the degradation of specific contact resistivity of Ag contact. Thus, the contact resistivity of Ag contact increased with increasing annealing temperature.

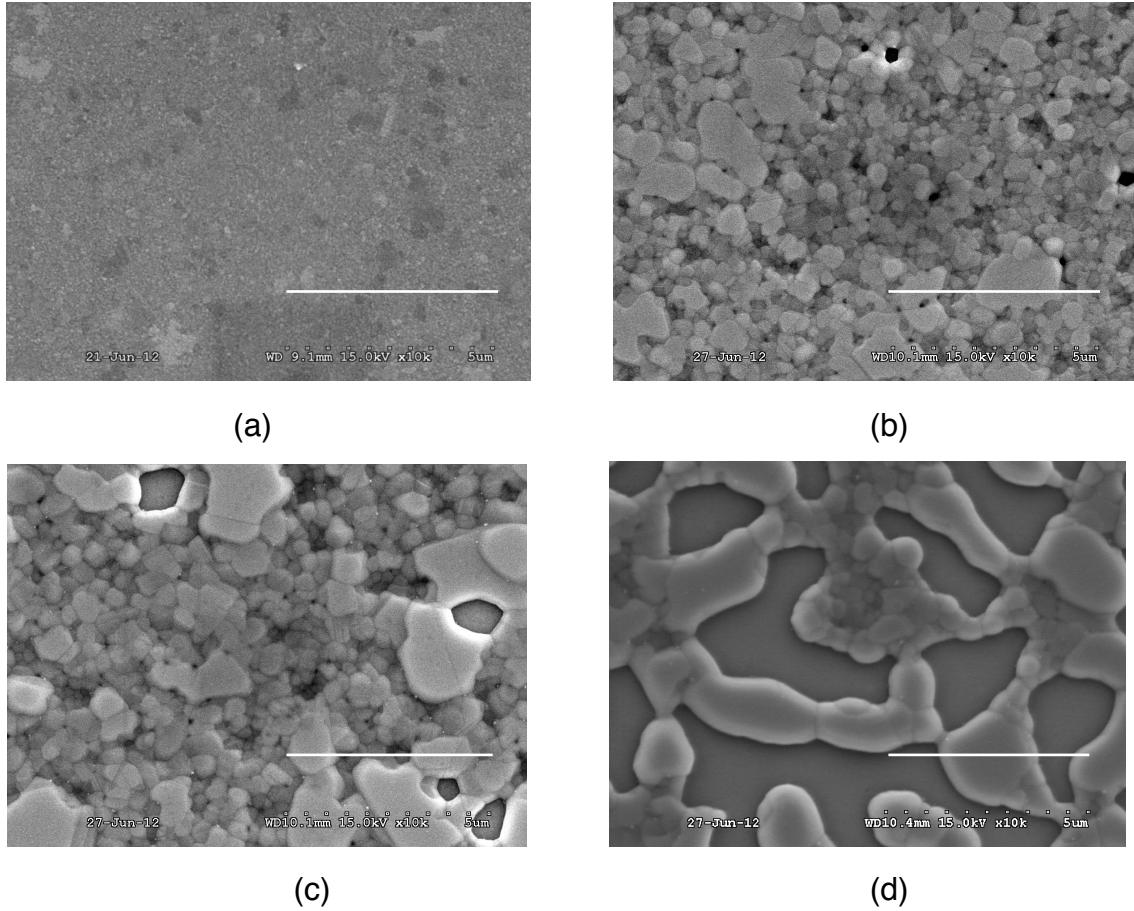


Figure 4.20: SEM images of Ag contacts annealed in oxygen for 2 minutes for the conditions of (a) as-deposited, (b) at 350 °C, (c) at 400 °C and (d) at 450 °C.

However, according to the CTLM I-V result shown in Figure 4.18 for Ag contact annealed in 2 and 10 minutes, the degradation of CTLM I-V for the 10 minutes annealing suggests that the agglomeration of Ag is not only dependent on the annealing temperature, but also dependent on the annealing time. Figure 4.21(a) illustrates the surface morphologies of Ag contact annealed for 10 minutes. It clearly shows that the agglomeration of the Ag contact surface was a lot more severer than that on the Ag contact sample annealed for 2 minutes at

450 °C illustrated in Figure 4.21(b). The Ag film had become isolated islands. Thus, the higher contact resistivity of Ag contact annealed in 10 minutes can be attributed to the severer Ag agglomeration reducing the effective contact area to p-GaN.

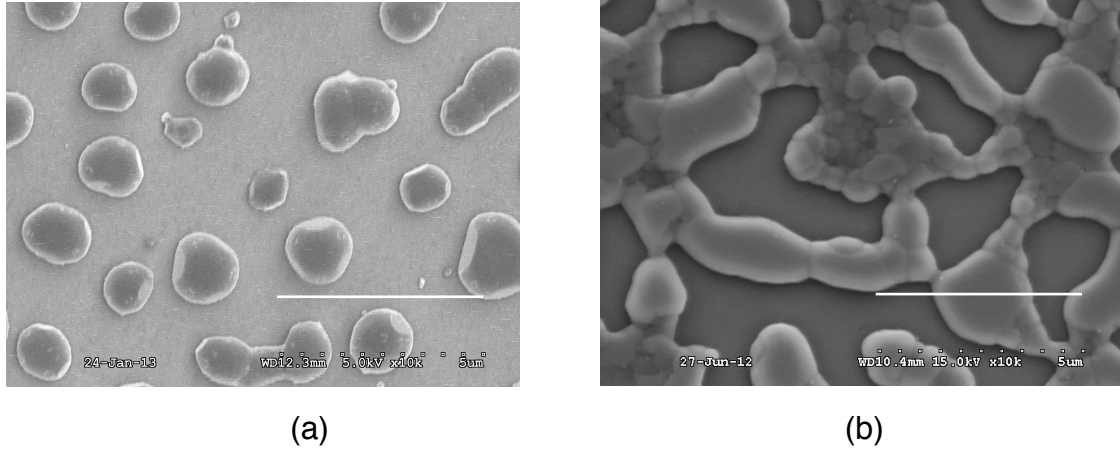


Figure 4.21: SEM images of Ag contacts annealed in oxygen at 450 °C for a) 10 minutes and b) 2 minutes.

Agglomeration of Ag thin film is a thermally activated process, which reduces the system free energy at high temperature by reducing the effective surface area of Ag film [19]. Thus, the reduction of the Ag film surface area and the stress generated during thermal annealing are likely to be the trigger for agglomeration. Ag agglomeration usually starts with grain boundary grooving, hillock and hole formations and eventually leading to agglomeration [20]. Grain boundary grooving originates from the surface diffusion of Ag atoms and this Ag atom surface diffusion is caused by the thermal stress and energy during annealing. It can be seen from Table 4.3 that Ag in the [111] crystal plane has the lowest surface free energy amongst all three orientations. Thus, Ag atoms in the Ag grains with plane orientation of [100] tend to diffuse to the grains with the orientation of [111], when the Ag film gains sufficient thermal energy during thermal treatment for atomic movements .

| Plane orientation | Surface free energy (J/m ²) |
|-------------------|---|
| [111] | 1.17 |
| [100] | 1.2 |
| [110] | 1.24 |

Table 4.3: Surface free energy of Ag with plane orientation of [111], [100] and [110] [21].

In addition, the Ag film is deposited on to the p-GaN surface and the thermal expansion coefficient of Ag ($18.9 \times 10^{-6}/\text{K}$) is significantly different from GaN ($5.6 \times 10^{-6}/\text{K}$). So a large compressive stress is induced when the Ag film is annealed. This compressive stress generally relaxes through grain boundary grooving. As a result, agglomeration of Ag occurs as illustrated in Figure 4.21(a). This thermal stress was calculated to be 6.4×10^8 Pa using the following equation.

$$S_T = \left(\frac{\alpha_f - \alpha_G}{1 - \nu} \right) E \Delta T \quad (4.11)$$

Where S_T is the thermal stress, α_f is the thermal expansion coefficient of Ag, α_G is the thermal expansion coefficient of GaN, ν is the poisson ratio of Ag, E is Young's modulus of Ag, ΔT is change of temperature.

In order to investigate the reflectance of the Ag contact, Ag (200 nm) films were deposited on to glass slides using an EBE. A spectrometer was then used to measure the reflectivity of the Ag contact. Figure 4.22 illustrates the reflectivity of the Ag contact as a function of annealing temperature. It can be seen that the Ag contact before thermal treatment had a very good reflectivity of 92 %. However, the reflectivity immediately dropped to 72 % after annealing at 350 °C, which can be attributed to the small voids on the contact surface due to agglomeration. It is apparent that the reflectivity significantly dropped from 67% to 55 % immediately after annealing at 450 °C. This can be attributed to the fact that the hole formation on the contact surface starts at 400 °C, which significantly reduces the contact coverage and hence reduces the reflectivity.

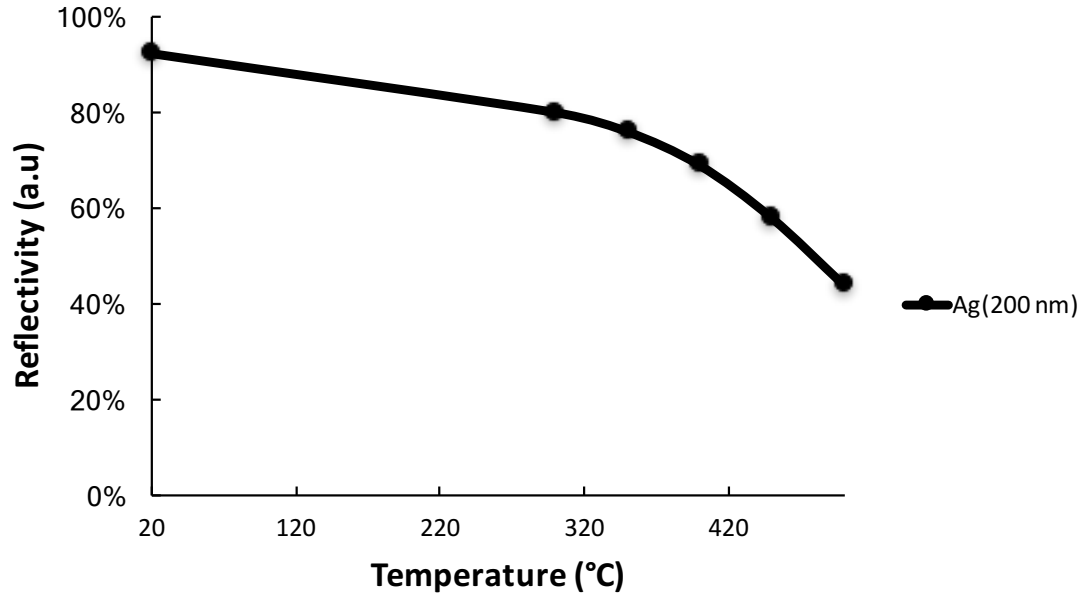


Figure 4.22: The reflectivity of Ag (200 nm) contact as a function of annealing temperature.

From the above investigations of Ag contact, annealing in oxygen for 2 minutes at 350 °C gave the lowest contact resistance to p-GaN. However, the Ag contact is not thermally stable and agglomerated during the high temperature treatment, leading to degradation in the contact resistivity and reflectivity. In principle, mitigating or preventing the Ag contact from agglomerating is the main factor that can improve the contact resistivity and reflectivity.

Since the Ag agglomeration originates from the diffusion of Ag atoms caused by the thermal stress generated during thermal treatment and the natural tendency of Ag atoms moving from [100] orientation to [111] orientation, suppressing the diffusion of Ag atoms from [100] to [111] orientation can reduce the Ag agglomeration. By inserting a thin layer of Ni as an interlayer between Ag and p-GaN layers has been reported to significantly reduce the number of grains with orientation of [100] in the Ag layer [22]. Therefore, using a bilayer contact scheme, i.e. Ni/Ag, can reduce Ag agglomeration.

In order to understand the impact of the layer thickness of the Ni interlayer, Ni/Ag contacts with layer thickness of 5 nm/200 nm and 1 nm/200 nm were deposited on the p-GaN. I-V measurements were performed on the CTLM test structure for the specific contact resistivity value. However, the I-V characteristics of both Ni/Ag (1 nm/200 nm) and Ni/Ag (5 nm/200 nm) contacts were not linear before annealing, as illustrated in Figure 4.23, due to again the Schottky barrier formed at the contact to p-GaN interface. As a result, a thermal treatment is also required.

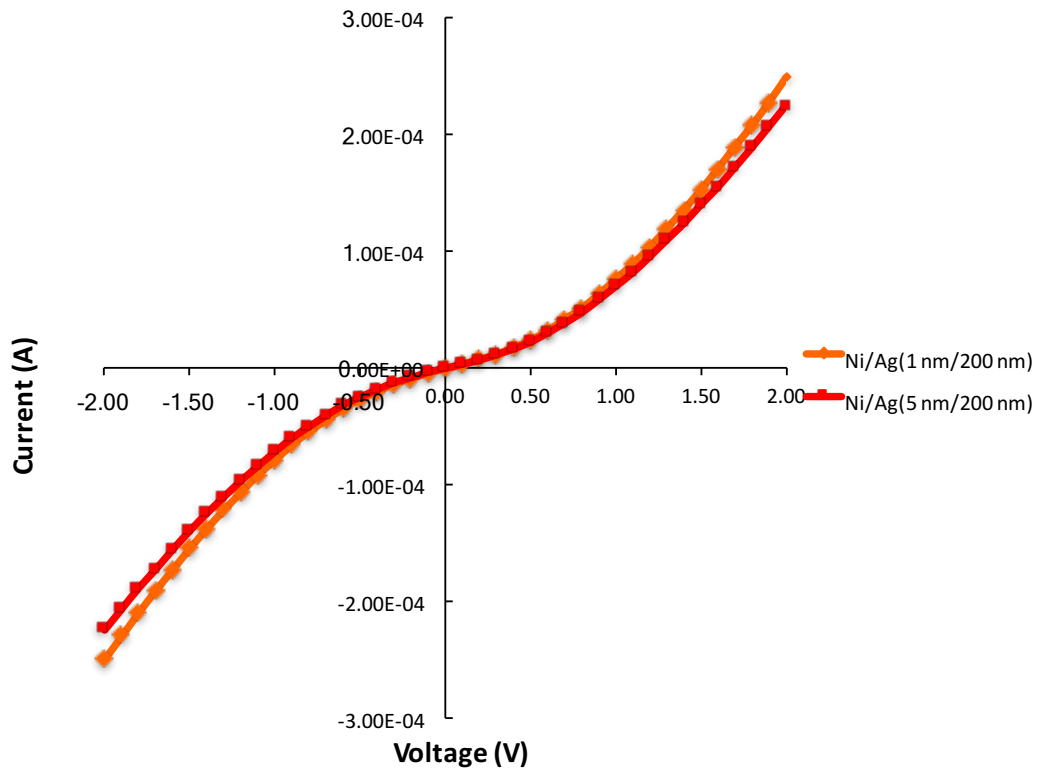


Figure 4.23: The I-V characteristics of Ni/Ag (1 nm/200 nm) & Ni/Ag (5 nm/200 nm) contacts before thermal treatment.

After annealing both Ni/Ag contact in oxygen for 2 minutes, the specific contact resistivity of both contacts was extracted from the measured I-V from the CTLM test structures. Figure 4.24 illustrates the specific contact resistivity of Ni/Ag (1 nm/200 nm) and Ni/Ag (5 nm/200 nm) and Ag (200 nm) contacts in the temperature range of 300 °C to 500 °C in a step of 50 °C in oxygen for 2 minutes.

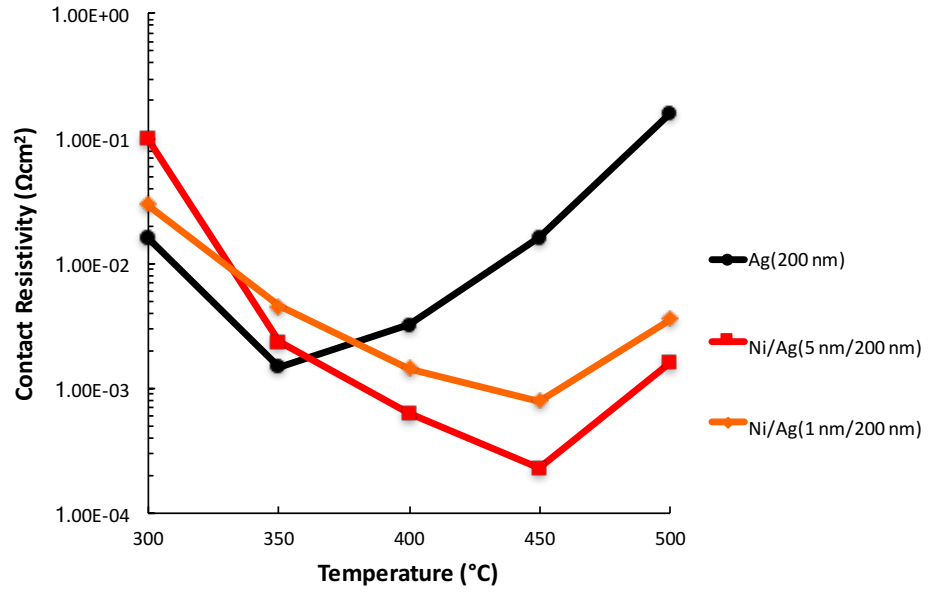
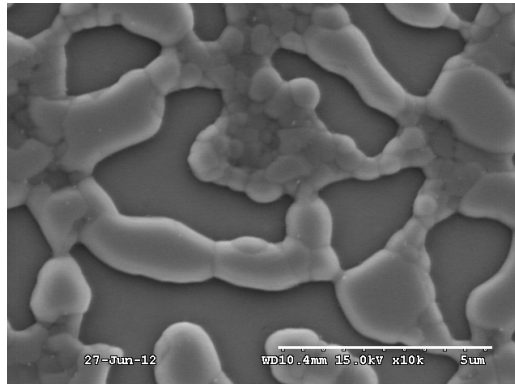
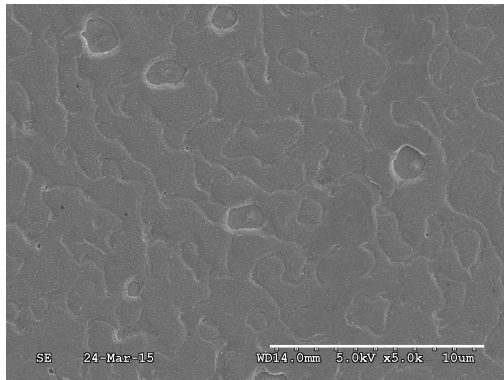


Figure 4.24: Specific contact resistivity of Ag (200 nm), Ni/Ag (1 nm/200 nm) and Ni/Ag (5 nm/200 nm) contacts as a function of annealing temperature.

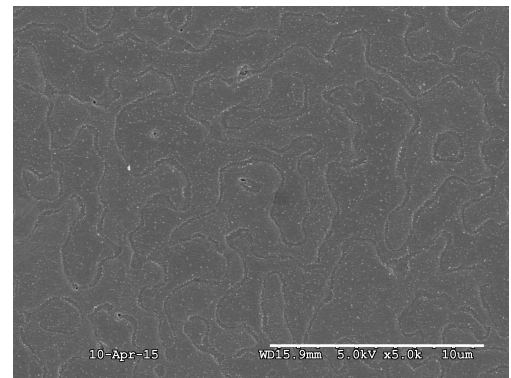
It can be seen that the contact resistivity of both Ni/Ag contacts showed a reducing trend as the annealing temperature increased until it reached 450°C. Both Ni/Ag contacts have the lowest contact resistivity at the annealing temperature of 450 °C, the values were $7.95 \times 10^{-4} \Omega\text{cm}^2$ for Ni/Ag (1 nm/200 nm) and $2.3 \times 10^{-4} \Omega\text{cm}^2$ for Ni/Ag (5 nm/200 nm). Furthermore, the contact resistivity of both Ni/Ag contacts was broadly lower than that of Ag-only contact annealing at 350 °C and it continued to reduce with increasing annealing temperature until it reached 450 °C. Figure 4.25 illustrates the surface morphologies of the Ag (200 nm), Ni/Ag (1 nm/200 nm) and Ni/Ag (5 nm/200 nm) after annealing at 450 °C for 2 minutes in oxygen. It can be seen that there were only a few voids and hillocks observed on the Ni/Ag (1 nm/200 nm) contact surface as shown in Figure 4.25(b). By using a thicker Ni interlayer, the Ni/Ag (5 nm/200 nm) contact showed an even smoother surface with almost undetectable voids and hillocks on the contact surface. Thus, the contact area of Ni/Ag contacts are not significantly reduced during high annealing temperature and allows the contact receptivity of Ni/Ag contact to remain low during high temperature thermal treatment.



(a)



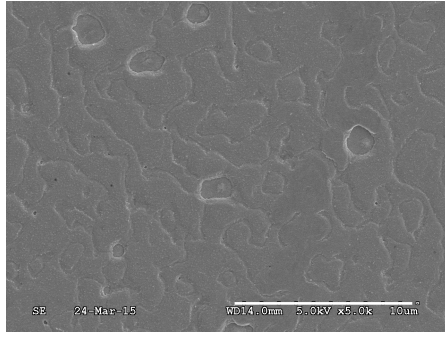
(b)



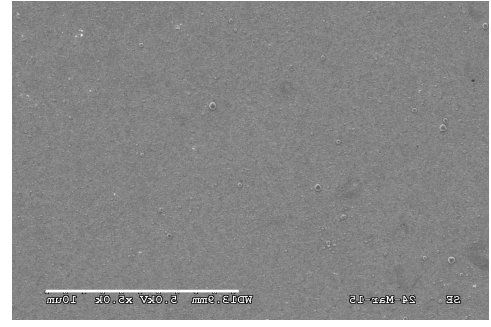
(c)

Figure 4.25: SEM images of a) Ag contact after annealed at 450°C, (b) Ni/Ag (1 nm/200 nm) after annealed at 450 °C and c) Ni/Ag (5 nm/200 nm) after annealed at 450 °C.

Although the agglomeration of the Ag contact was significantly reduced by inserting a thin layer of Ni interlayer. However, a small amount of voids was still observed. Since the Ag agglomeration was mentioned above due to the Ag surface atomic movement during the thermal treatment, this surface movement can be suppressed if a thin layer of Ni is deposited on top of the Ni/Ag contact as a capping layer. Figure 4.26 illustrates the SEM images of Ni/Ag/Ni (1 nm/200 nm/10 nm) and Ni/Ag (1 nm/200 nm) contact surface topologies annealed at 450 °C for 2 minutes in oxygen environment. By capping the Ni/Ag (1 nm/200 nm) contact with a thin 10 nm Ni layer, the void formation was not observed. This can be attributed to the suppression of Ag surface atomic movement.



(a)



(b)

Figure 4.26: SEM images of (a) Ni/Ag (1 nm/200 nm) after annealed at 450 °C and (b) Ni/Ag/Ni (1 nm/200 nm/10 nm) after annealed at 450 °C.

Figure 4.27 illustrates the contact resistivity of the Ag-based contact to p-GaN in the annealing temperature range of 300 °C to 500 °C. By capping the Ni/Ag with 10nm Ni showed a very pronounced effect of improving the specific contact resistivity. It can be seen that the contact resistivity of Ni/Ag/Ni contact is $6.3 \times 10^{-5} \Omega\text{cm}^2$ for the annealing temperature of 450 °C, which is the lowest among all other contacts. This can be attributed to the suppression of Ag agglomeration.

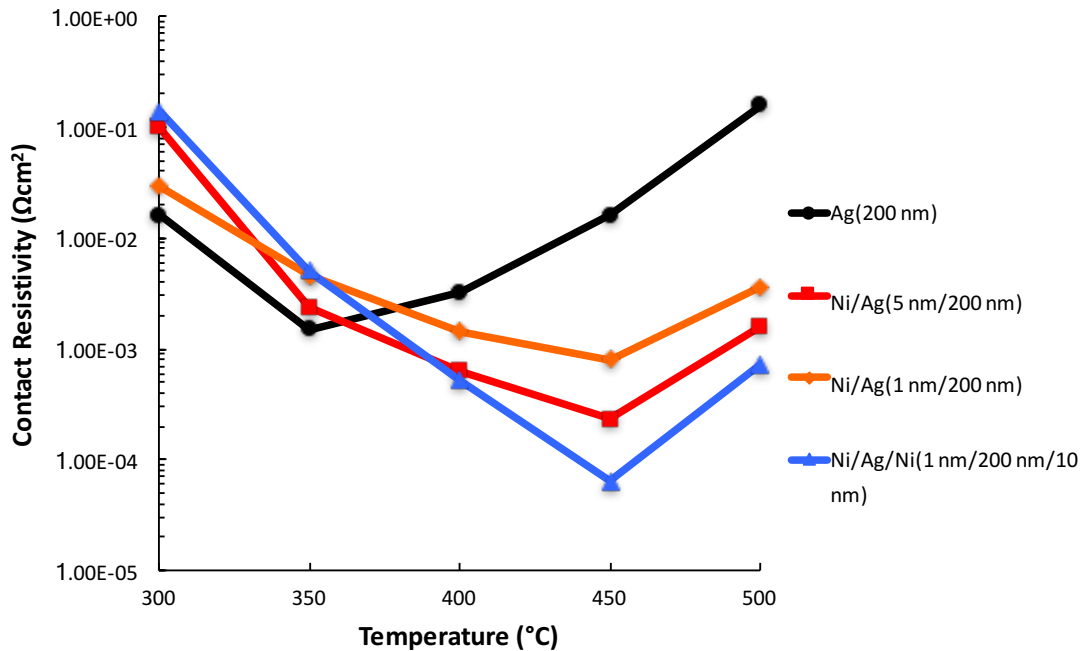


Figure 4.27: The specific contact resistivity of Ag (200 nm), Ni/Ag (1 nm/200 nm), Ni/Ag (5 nm/200 nm) and Ni/Ag/Ni (1 nm/200 nm/10 nm) as a function of annealing temperature.

Figure 4.28 compares the reflectivity of the Ag (200 nm), Ni/Ag (1 nm/200 nm), Ni/Ag (5 nm/200 nm) and Ni/Ag/Ni (1 nm/200 nm/10 nm) contacts as a function of annealing temperature. It is well known that Ag is a very good reflector and can be seen in the result that the Ag contact before annealing showed a reflectivity of 92 %. However, it experienced a strong agglomeration and formed holes on the contact surface during annealing in oxygen. As a result, its reflectivity was reduced to 44 % after annealing at 500 °C. It was found that the reduction of reflectivity of the Ag contact was mitigated by adding a thin 1nm Ni interlayer. The Ag-only contact experienced a strong 23 % of reflectivity degradation immediately after annealing at 400 °C (i.e. reflectivity reduced from 92 % to 69 %). While the Ni/Ag (1 nm/200 nm) only experienced a 11 % reflectivity degradation, (i.e. reflectivity reduced from 85 % to 74%), and also gave a better contact specific resistivity. This result suggests that having less voids and holes on the contact surface not only can improve the specific contact resistivity, but also improve the reflectivity. However, increasing the Ni layer thickness caused a reduction in the reflectivity. Ni/Ag (5 nm/200 nm) showed the lowest reflectivity (i.e. 65 %), at the as deposited state. This result suggests that Ni acts as a light absorption layer and thick Ni layer can result in large absorption causing a low contact reflectivity. By putting a 10nm Ni capping layer above the Ni/Ag (1 nm/200 nm/10 nm) was able to prevent the reflectivity degradation during the thermal treatment. Its thermal stability was the best amongst all four contacts. It hardly experienced reflectivity degradation after thermal treatment and the reflectivity only reduced by 12 % after 500 °C annealing to 73 %. In addition, it provided the lowest specific contact resistivity, i.e. $6.3 \times 10^{-5} \Omega \text{cm}^2$, after annealing at 450 °C. These results also suggest that the better the suppression of Ag agglomeration is, the better the contact resistivity and reflectivity.

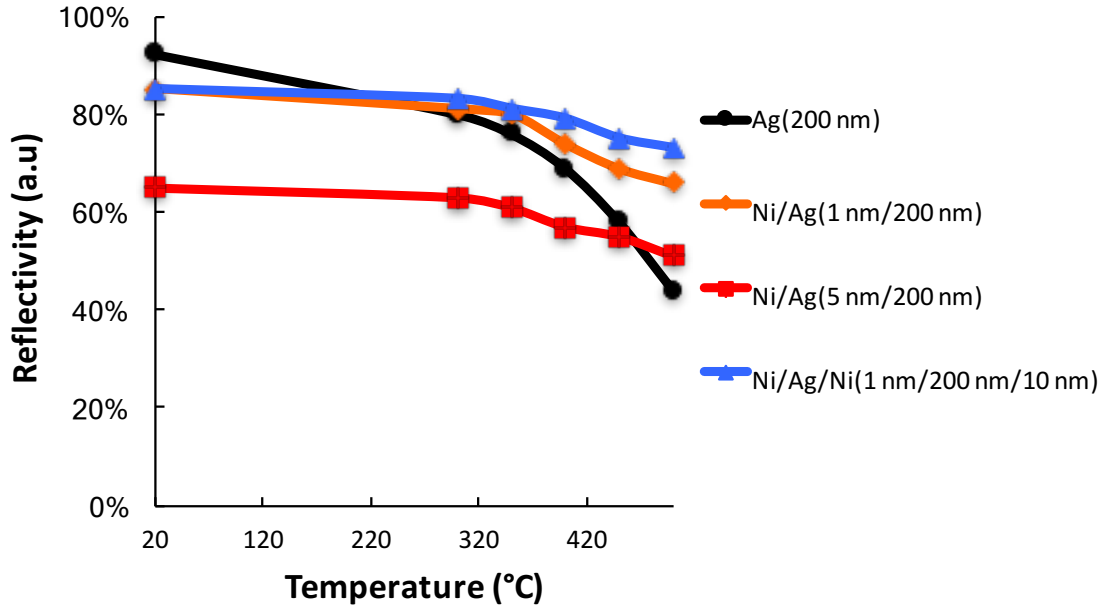


Figure 4.28: The reflectivity of Ag (200 nm), Ni/Ag (1 nm/200 nm) and Ni/Ag (5 nm/200 nm) contacts as a function of annealing temperature.

In order to investigate the impact of these contacts on the light output of fully fabricated VLED devices, VLEDs with Ag (200 nm), Ni/Ag (1 nm/200 nm) and Ni/Ag (5 nm/200 nm) p-type contacts were fabricated and the light output power of these LED samples were measured using an integrating sphere. Figure 4.29 illustrates the light output characteristics of Ag (200 nm) contact annealed at 350 °C, Ni/Ag (1 nm/200 nm), Ni/Ag (5 nm/200 nm) and Ni/Ag/Ni (1 nm/200 nm/10 nm) contacts annealed at 450 °C as a function of drive current. It can be seen that the Ni/Ag/Ni contact had 23 mW and 52 mW of light output power, which is the highest amongst all four contacts at the drive current of 100 mA and 300 mA respectively. Comparing this result to the VLEDs without any reflectors fabricated by Xiong et. al., their VLED light output power is only 3.5 mW at 100 mA [23]. This is approximately 20 mW lower than our VLED using Ni/Ag/Ni as the reflector. It is worth noting that Ni/Ag (1 nm/200 nm) contact showed a 42 mW of light output power, which is higher than that of Ni/Ag (5 nm/200 nm) contact at the drive current of 300 mA. Although the Ni/Ag (5 nm/200 nm) had a lower contact resistivity compared to Ni/Ag (1 nm/200 nm) and Ag (200 nm) contacts, its light output is still lower than the VLED with Ni/Ag (1 nm/200 nm) sample and Ag-only sample. This result suggests that the contact reflectivity has a greater impact on the LED light output than contact resistivity

and also indicates that Ni/Ag/Ni (1 nm/200 nm/10 nm) contact is the best reflector candidate amongst all four contact investigated.

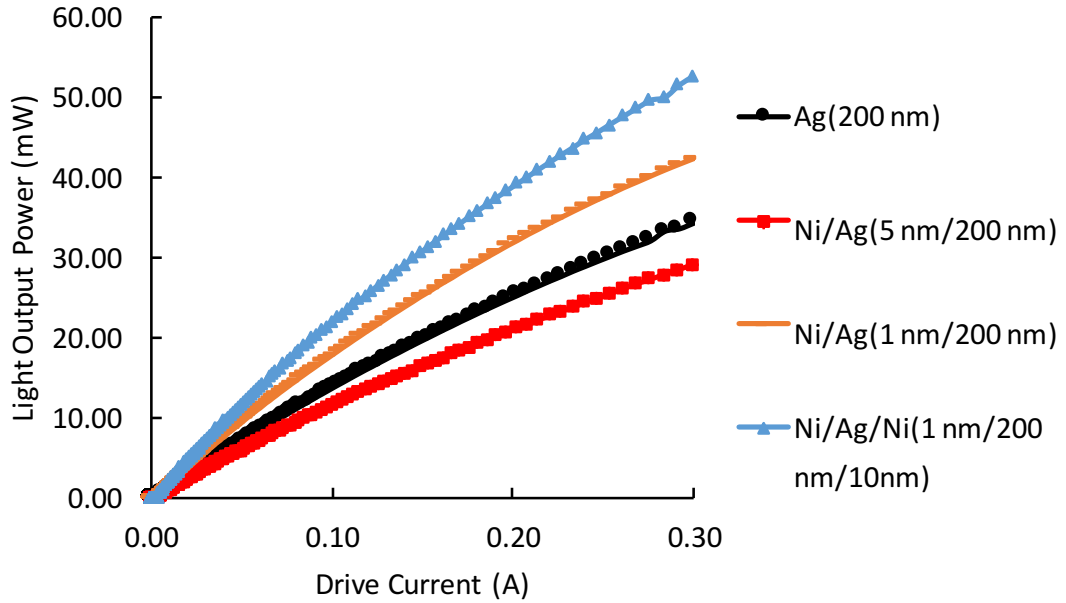


Figure 4.29: Light output of LED samples fabricated with Ag (200 nm) annealed at 350 °C for 2 minutes, Ni/Ag (1 nm/200 nm), Ni/Ag (5 nm/200 nm) and Ni/Ag/Ni (1 nm/ 200 nm/10 nm) contacts annealed at 450 °C for 2 minutes as a function of drive current.

Figure 4.30 illustrates the I-V characteristics of LED samples fabricated with Ag (200 nm), Ni/Ag (1 nm/200 nm), Ni/Ag (5 nm/200 nm) and Ni/Ag/Ni (1 nm/200 nm/10 nm) as the p-type ohmic contacts, which were annealed at 350 °C for Ag-only and 450 °C for the rest in oxygen environment. It clearly shows that the LED sample with Ag (200 nm) contact had the worst I-V characteristic amongst all four contacts due to its higher contact resistivity. It required an operation voltage of 9.8 V at the drive current of 300 mA. In contrast, the sample with Ni/Ag/Ni (1 nm/200 nm/10 nm) showed the best I-V characteristics compared to the other contacts. It only required an operation voltage of 2.99 V and 4.95 V at the injection current of 20 mA and 300 mA respectively. Comparing this result to the VLEDs fabricated by Xiong et. al., their VLED forward is only 2.5 V at 20 mA [23]. The forward voltage of our VLED with Ni/Ag/Ni contact is approximately 0.5 V higher. This can be attributed to our Si carrier substrate being not thinned down to 100 μm . It is worth noting that the Ni/Ag (1 nm/200 nm) and Ni/Ag (5 nm/200 nm) required a forward voltage of 5.7 V and 7.4 V under the same current level. The reduction of Ni/Ag (5 nm/200 nm) contact in the forward voltage can be attributed to the lower specific contact resistivity value due to the

suppression of Ag agglomeration. This result suggests that making a good ohmic contact to p-GaN is very important as a better ohmic contact behaviour can reduce the operation voltage.

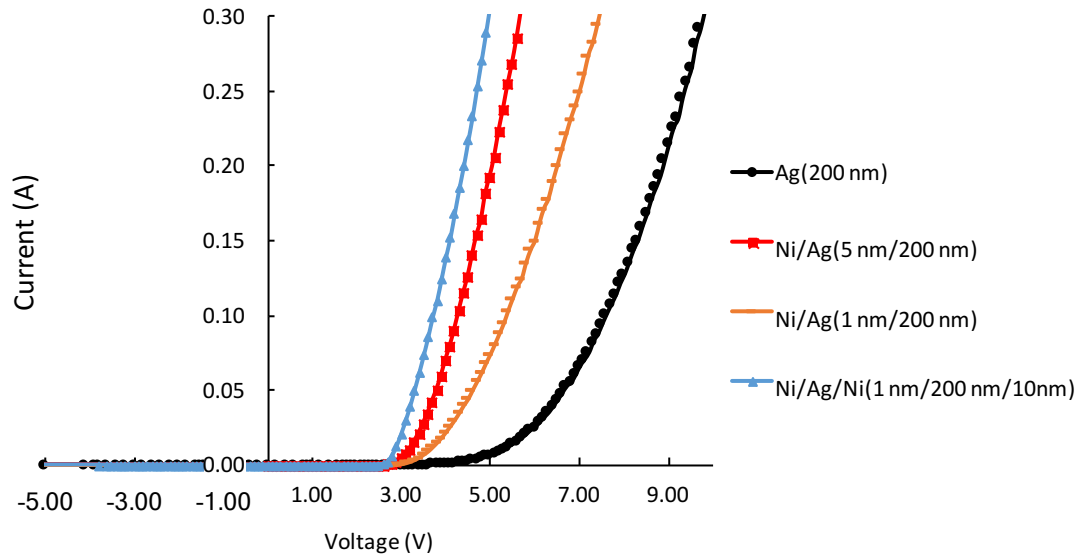


Figure 4.30: *I-V characteristics of LED samples fabricated with Ag based p-type contacts.*

Figure 4.31 illustrates the wall-plug efficiencies (WPEs) of VLEDs fabricated with the Ag-based contacts as a function of drive current. It can be clearly seen that the Ni/Ag/Ni contact showed 36 mW/W of WPE at 300 mA of drive current, which is the highest amongst all other contacts. It is worth noting that although Ag contact showed a higher light output power than that of Ni/Ag (5 nm/200 nm), the WPE of Ag contact is 4 mW/W lower than the Ni/Ag contact. This can be attributed to the excess power consumed on the contact due to high contact resistivity.

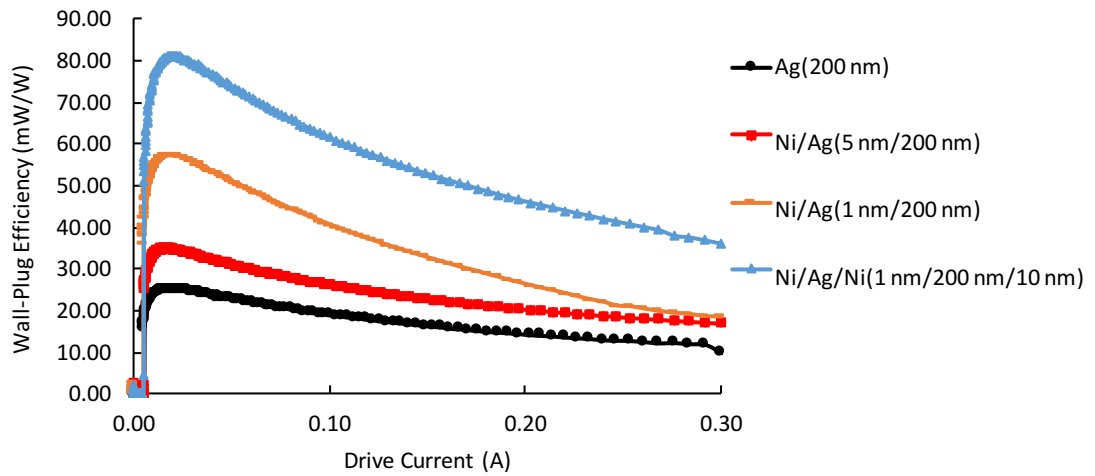


Figure 4.31: *The wall-plug efficiencies of VLED fabricated with Ag (200 nm), Ni/Ag (1 nm/200 nm), Ni/Ag (5 nm/200 nm) and Ni/Ag/Ni (1 nm/200 nm/10 nm) contacts.*

4.8.Conclusion

This work has developed a reflective low resistant Ni/Ag/Ni ohmic contact to p-GaN. Ag is a highly reflective material in the visible spectrum. Since an as-deposited Ag layer only make a Schottkly contact to p-GaN, a thermal treatment in oxygen environment is required to make Ag become a good ohmic contact. Annealing the contact in oxygen can promote Ga atoms to out-diffuse to the Ag layer and form Ga-Ag solid solution. The out-diffused Ga atoms can act as acceptors. As a result, the surface hole concentration of p-GaN layer increases, reducing the space charge region width. This width reduction can significantly increase the probability of hole tunnelling occurring and leads to the formation of ohmic contact. A specific contact resistivity as low as $1.5 \times 10^{-3} \Omega \text{cm}^2$ can be achieved by annealing the Ag (200 nm) contact in oxygen environment for 2 minutes at 350 °C. However, the plain Ag contact is not thermally stable and experiences severe degradation of its electrical and optical properties during thermal treatment due to Ag agglomeration. Thus, its contact resistivity and reflectivity degrade to $1.5 \times 10^{-1} \Omega \text{cm}^2$ and 44 % respectively after annealing at 500 °C. It was found that this agglomeration problem can be mitigated by inserting a thin Ni interlayer between the Ag layer and p-GaN layer. This is because Ni interlayer can reduce the grains with [100] orientation in the Ag layer, reducing the surface diffusion of Ag atoms to [111] oriented grains. As a result, the Ag agglomeration is suppressed. The specific contact resistivity as low as $2.3 \times 10^{-4} \Omega \text{cm}^2$ for Ni/Ag (5 nm/200 nm) and $7.95 \times 10^{-4} \Omega \text{cm}^2$ for Ni/Ag (1 nm/200 nm) can be achieved by annealing both contacts in oxygen for 2 minutes at 450 °C. Although the Ag contact with 5nm Ni interlayer had the lowest contact resistivity, its reflectivity is 15 % worse than the Ni/Ag (1 nm/200 nm) contact after annealing at 450 °C. It is worth noting that LEDs fabricated with Ni/Ag (5 nm/200 nm) and Ni/Ag (1 nm/200 nm) contacts showed 29 mW and 42 mW of light output power with a forward voltage of 5.7 V and 7.4 V at 300 mA drive current, respectively. This results suggest that light output power is dominated by the reflectivity and not the contact resistivity. It was found that the the Ag agglomeration in the Ni/Ag (1 nm/200 nm) can be further suppressed by capping the Ni/Ag with 10nm Ni on top. The resultant Ni/Ag/Ni (1 nm/200 nm/ 10 nm) was very thermally stable and formed a very good ohmic contact to p-

GaN. It was able to achieve a contact resistivity as low as $6.3 \times 10^{-5} \Omega \text{cm}^2$ and the reflectivity still remained above 80 % (ie. 83 %) after annealing in oxygen for 2 minutes. As a result, the LED fabricated with Ni/Ag/Ni (1 nm/200 nm/10 nm) showed the best light output power and operational voltage. It only required a forward voltage of 4.95 V to conduct 300 mA and produce a 52 mW of light output power. In addition, The light output power of our VLEDs using Ni/Ag/Ni contact is approximately 20 mW higher than the VLEDs fabricated by Xiong et. al. at 100 mA. Although our forward voltage at 20 mA is 0.5 V higher than the VLEDs fabricated by Xiong et. al., it can be attributed to our Si carrier substrates without any thickness reduction process.

4.9.References

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Chapter 5

Investigation of Ni/Au/Ag-based contact

5.1.Introduction

The electrical contacts on GaN-based light emitting diodes (LEDs) are usually made of thin multiple layers of metals designed to provide a low electrical resistance interface between the power source and the GaN contact layer, with ideally no potential barrier or changes to the current to voltage (I-V) performance of epitaxial structure. Therefore, a great care must be taken in designing ohmic contacts and the processes used in their fabrication. It was mentioned in the previous chapter that ohmic contacts to p-GaN are difficult to form. This is because metals with work function higher than p-GaN ($\Phi_{\text{p-GaN}} = 6.5$ eV) [1] are difficult to find. Also, it is very challenging to achieve p-GaN with high doping density (i.e. hole concentration $> 1 \times 10^{18} \text{ cm}^{-3}$) [2]. A high optically reflective Ni/Ag ohmic contact with low contact resistivity was developed in chapter 4. It was found that by inserting a thin layer of Nickel (Ni) layer can significantly reduce the contact resistivity and preserve the contact reflectivity. However, the silver (Ag) mirror contact inevitably degrades during the short annealing process as the Ag mirror must be annealed together with the Ni layer in order to form an ohmic contact.

It was found that Ni/Ag contacts have been widely used and accepted as the standard p-GaN ohmic contact for flip-chip LEDs grown on sapphire substrates due to its ability to achieve a moderate contact resistivity (as low as $2.3 \times 10^{-4} \Omega \text{cm}^2$) by increasing the hole concentration in the adjacent p-GaN layer by creating Ga vacancies after the short duration thermal treatment [3, 4]. Further, Ag has a theoretical optical reflectivity of ~95 % at the wavelength of 470 nm making it a good choice as a reflector contact. However, thin film Ag contacts are not thermally stable and can easily agglomerate at even moderate temperatures due to its poor chemical adhesion to p-GaN [5-7]. Although a thick

Ag film (i.e. $\sim 1 \mu\text{m}$) can be used to mitigate agglomeration, it adds extra manufacturing cost [8]. During the wafer bonding process of the vertical LEDs (VLEDs) the p-type contact is exposed to temperatures typically in the range of 250°C to 450°C for up to 30 minutes [9-11] with the effect that either the contact resistivity or the reflectivity, or both may be degraded. As a consequence, this thermal instability issue is more critical for GaN grown on Si-VLED technology as the p-contact must be able to retain its high reflectivity to prevent loss in the bonding metals and carrier substrate whilst retaining low contact resistance after the high temperature wafer bonding process (WBP).

Ni/Au has been widely used as a p-type transparent contact layer (TCL) for lateral contact LEDs that emit light through the p-type GaN layer. After annealing in air, an Ni/Au contact has a high transmittance of 88 % in the blue spectrum range [12] and has the ability to form a very low contact resistivity of $4 \times 10^{-6} \Omega\text{cm}^2$ [13]. Although the Ni/Au contact has such a good contact resistivity, it cannot be used straight forwardly in VLED due to its poor reflectivity. To date, the possibility of combining the merits of the optical reflectivity of an Ag thin film with the low contact resistivity of Ni/Au contacts in obtaining a high reflectivity and low resistance Ohmic contact for a VLED has received little attention. However, concerns remain that the scope for achieving simultaneously low contact resistance and high optical reflectivity may be compromised by the trend to higher temperature wafer bonding processes, to improve LED packaging reliability, gives rise to concerns about the integrity and the stability of reflecting contacts on p-type GaN.

In this chapter, the electrical and optical stability of Ni/Au/Ag-based contacts will be investigated by annealing these contacts at 450°C for 30 minutes under air ambient to simulate the worst-case scenario of a wafer bonding process. The blue emission InGaN/GaN grown on Si VLEDs test structures have been fabricated and characterized, to investigate the impact of the Ni/Au/Ag-based contacts on the performance of fully fabricated devices.

5.2.Experimental Details

A 6-inch diameter InGaN/GaN LED epitaxy grown on Si substrate by metallorganic chemical vapour deposition (MOCVD), was provided by Plessey Semiconductor Ltd. This wafer has a 650 nm AlGaIn buffer layer, a 1470 nm thick n-GaN, 6 pairs of InGaN/GaN multiple quantum wells (MQWs) with a total thickness of 200 nm and 95 nm of p-GaN. To examine the p-type specific contact resistivity (ρ_c), circular transmission line model (CTLTM) test structures and a p-type contact pattern were defined on the p-GaN using photolithography for a subsequent lift-off. The CTLTM has nine test points and spacing between the cutouts and inner contact pads are 3, 5, 10, 15, 20, 30, 50, 85 and 120 μm (see Chapter 3).

A 3 nm thick Ni layer and 3 nm thick Au layer were then deposited by using electron beam evaporation (EBE) without breaking the vacuum. The resulting structure was then subjected to a rapid thermal annealing (RTA) treatment at 500 °C for 5 minutes to form an Ohmic TCL. Next, different combinations of Ni and Ag layers, as tabulated in Table 5.1, were deposited, again using EBE, on top of the Ni/Au TCL to act as the mirror. These samples were then annealed at 450 °C for 30 minutes in air ambient in a furnace to simulate the worst-case scenario wafer bonding condition. Bonding metals of Ti/Ni/Sn/Au (200 nm/100 nm/1700 nm/50 nm) and Ti/Pt/Ag/Au (200 nm/100 nm/3500 nm/50 nm) were deposited by EBE the Si carrier substrate and on top of Ni/Au/Ag based contacts on the LED wafers respectively. The LED sample and the Si carrier substrate were then put in contact for the wafer bonding process, which was carried out at 260 °C for 30 minutes. The reflectance of the Ni/Au/Ag-based samples was measured using a spectrophotometer. The light output-current-voltage characteristics of the VLEDs were measured under 10ms pulsed conditions (to minimize self-heating) on-wafer using a current-voltage source unit (Keithley 2600) with an integrating sphere instrument placed 3 mm above the wafer surface over low-profile electrical probes.

| Metallization scheme | Thickness (nm) |
|----------------------|----------------|
| Ni/Ag | 1/200 |
| Ni/Au/Ag | 3/3/200 |
| Ni/Au/Ni/Ag | 3/3/1/200 |
| Ni/Au/Ni/Ag/Ni | 3/3/1/200/10 |

Table 5.1: Metal contact thickness for LED and p-GaN samples.

5.3. Results and Discussions

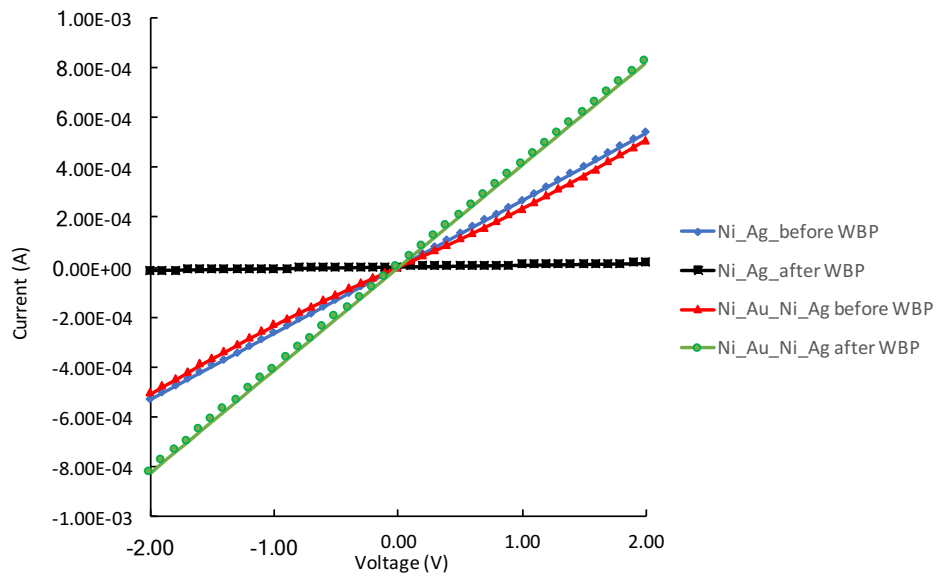


Figure 5.1: I-V characteristics of CTLM test structure on Ni/Ag and Ni/Au/Ni/Ag contacts before and after the simulated wafer bonding process.

In order to evaluate the electrical parameters of the contact, the I-V characteristics of a CTLM test structure of Ni/Ag (1 nm/200 nm) and Ni/Au/Ni/Ag (3 nm/3 nm/1 nm/200 nm) contacts before and after experiencing the simulated WBP were measured. The results are compared in Figure 5.1. It can clearly be seen that the 450 °C, 30 minute annealing does not have a direct impact on the linearity of I-V characteristics of the Ni/Au/Ni/Ag and Ni/Ag contact schemes. However, the slope of the I-V characteristics of the Ni/Ag (1 nm/200 nm) contact is greatly reduced after the simulated WBP, only conducting 1.52×10^{-5} A at 2 V. On the other hand, inserting the Ni/Au TCL underneath the Ni/Ag layers, the resultant Ni/Au/Ni/Ag contact could conduct 5.06×10^{-4} A and 8.21×10^{-4} mA at 2 V, before and after the wafer bonding process respectively. Thus, the electrical

degradation was prevented by the underlying Ni/Au layers indeed the contact became even more conducting afterwards.

| Contact | Ni/Ag | Ni/Au/ Ag | Ni/Au/Ni/ Ag | Ni/Au/Ni/ Ag/Ni |
|---|-----------------------|-----------------------|-----------------------|-----------------------|
| ρ_c before WBP [Ωcm^2] | 4.79×10^{-4} | 1.35×10^{-3} | 3.03×10^{-3} | 3.93×10^{-3} |
| ρ_c after WBP [Ωcm^2] | 2×10^{-1} | 1.08×10^{-3} | 1.56×10^{-5} | 1.38×10^{-5} |

Table 5.2: The specific contact resistivity (ρ_c) of the ohmic contact before and after the simulated WBP.

The specific contact resistivity ρ_c of various contact structures before and after the simulated WBP are compared in Table 5.2. As can be seen, after carrying out the simulated WBP, the ρ_c of all the Ni/Au/Ag-based contacts were improved, whereas the ρ_c of the Ni/Ag contact degraded by more than two order of magnitude. This clearly shows that the combination of Ag mirror with the Ni/Au TCL forms a much more thermally stable Ohmic contact with very low contact resistance.

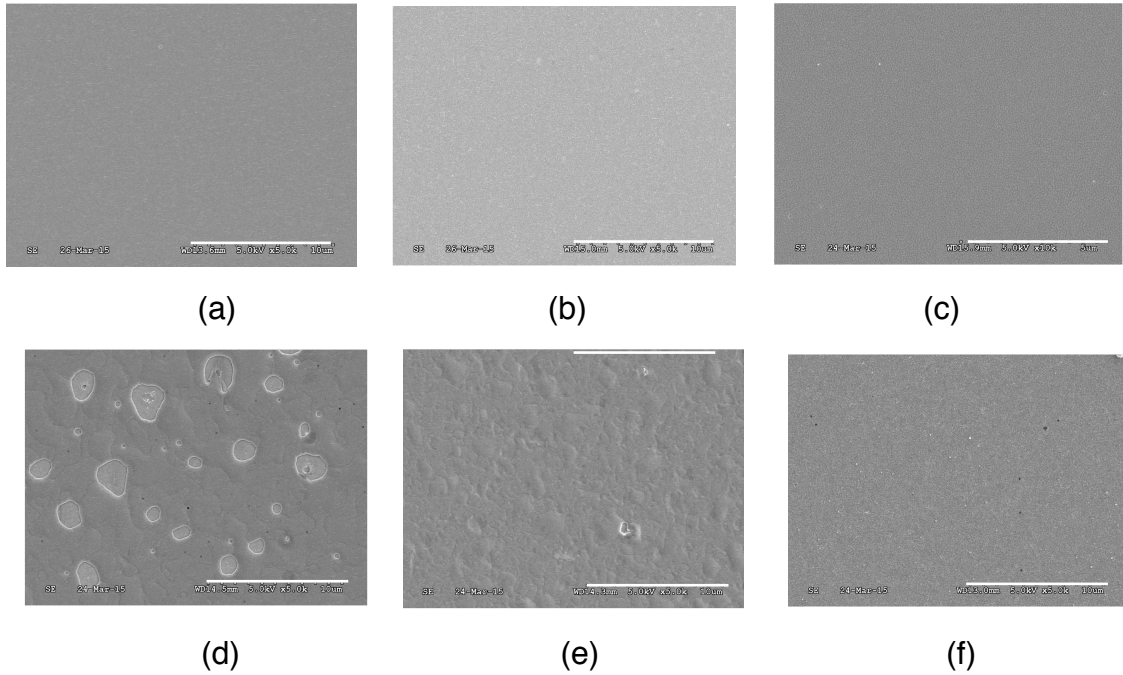


Figure 5.2: The SEM SE top view images of (a) Ni/Ag, (b) Ni/Au/Ni/Ag and (c) Ni/Au/Ni/Ag/Ni contacts after the deposition, and (d) Ni/Ag, (e) Ni/Au/Ni/Ag and (f) Ni/Au/Ni/Ag/Ni contacts after the simulated wafer bonding process.

The surface morphology of a metal contact can also play an important role as it can have an impact on the electrical and optical stabilities. Figure 5.2 shows scanning electron microscopy (SEM) images of the surface morphology of Ni/Ag, Ni/Au/Ag, Ni/Au/Ni/Ag and Ni/Au/Ni/Ag/Ni contacts after the simulated WBP. The plain Ni/Ag contact shows an irregular surface morphology with voids formed in the Ag layer owing to agglomeration of the latter. Ag agglomeration is a thermally activated process, which reduces the surface area of the Ag contact film to the underlying GaN layer interface area via atomic surface diffusion [14]. Since the Ag film has a poor adhesion to the underlying p-GaN surface and a high surface to volume ratio, it can easily degrade through agglomeration. It can be seen from Figure 5.2(b) that, by inserting a Ni/Au TCL as an interlayer between the Ag mirror and the p-GaN layer, Ag agglomeration was reduced due to the reduction of atomic surface diffusion on the underlying Ni/Au TCL. Ag agglomeration was further reduced by adding another thin layer of Ni on top of the Ni/Au TCL. Figure 5.2(c) shows that virtually no voids form in the Ag layer in Ni/Au/Ni/Ag contact in contrast to Ni/Ag or Ni/Au/Ag contacts. This is in agreement with well-established result that Ni inhibits Ag agglomeration: the strategy, as demonstrated here, is to have the Ag directly in contact with Ni which acts as a wetting layer. Thus, a further 10 nm thick Ni has been added to sandwich the 200 nm thick Ag layer to form a Ni/Au/Ni/Ag/Ni stack. The upper Ni layer also prevents the Ag mirror from being oxidized or react with hydrogen sulphide during any thermal treatments such as the WBP or lifetime tests. It can also act as a capping layer to suppress the Ag agglomeration. This contact scheme was found to be the most effective from the perspective of void formation, as none were observed after the simulated WBP.

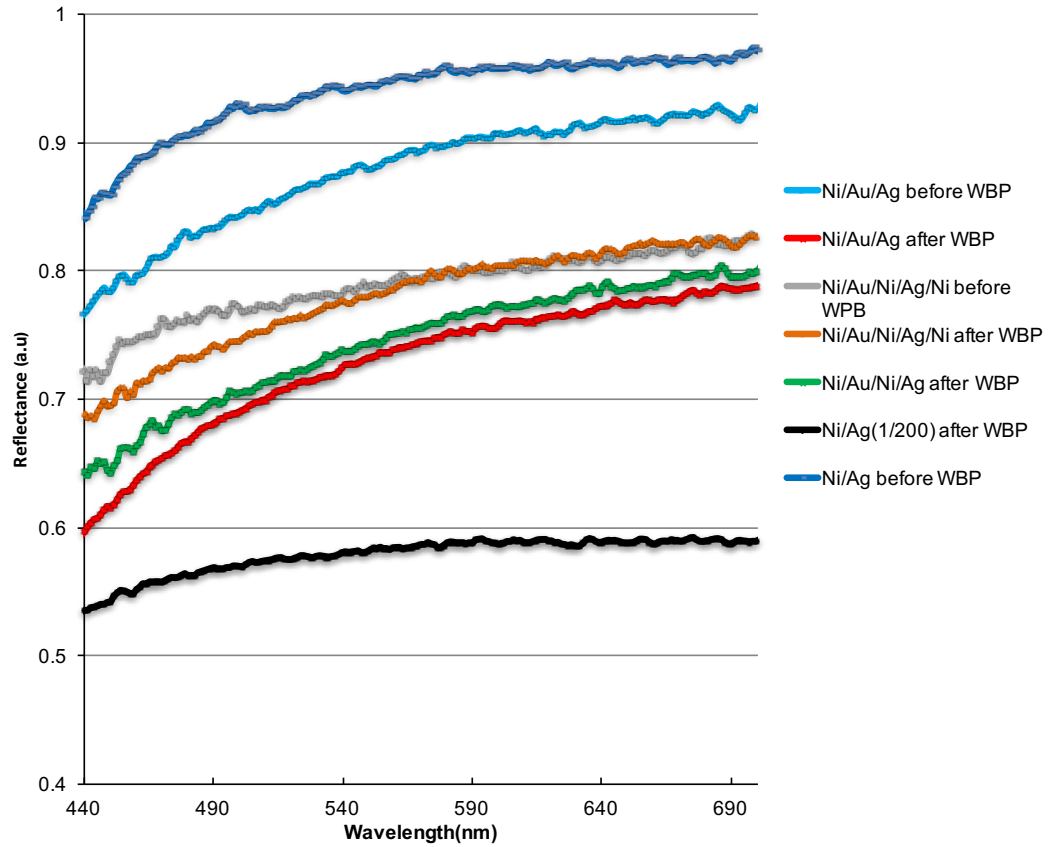


Figure 5.3: Comparison of the reflectance of Ni/Ag, Ni/Au/Ag, Ni/Au/Ni/Ag and Ni/Au/Ni/Ag/Ni contacts before and after the simulated wafer bonding process.

Figure 5.3 compares the reflectivity of the Ni/Ag and Ni/Au/Ag-based contacts before and after the simulated WBP as a function of wavelength. Before the simulated WBP, the Ni/Ag contact had a reflectivity of 88 % at the wavelength 470 nm, as can be seen in Figure 5.3, which was the highest among all contacts. The Ni/Au/Ag contact had a reflectivity of 81 % and the Ni/Au/Ni/Ag and Ni/Au/Ni/Ag/Ni contacts both showed a reflectivity of 76 % at the wavelength of 470 nm before the simulated WBP. Although the TCL of Ni/Au was very thin and highly transparent, it still degraded the reflectivity of Ag mirror, as expected. As seen in Figure 5.3, the long 30 minute simulated WPB at 450 °C significantly degraded the reflectivity of Ni/Ag contact to 57 %. This can be attributed to the reduction of reflective area of the contact due to Ag agglomeration, as seen in the SEM image of Ni/Ag after the WPB (i.e. Figure 5.2(d)). However, the Ni/Au/Ag-based contact did not exhibit a serious optical degradation and the reflectivity of Ni/Au/Ag and Ni/Au/Ni/Ag contacts only dropped to 65 % and 69 % respectively. This can be attributed to the reduction of agglomeration. By adding a thin layer of Ni overlay on the Ag mirror, the

reflectivity of the Ni/Au/Ni/Ag/Ni contact only exhibited a minimal degradation, reducing the reflectivity to 69 %, a relative reduction of just 9 % induced by the simulated WBP. This can clearly be attributed to the Ni overlay inhibiting the atomic diffusion of the Ag mirror, leading to a void-free surface as seen in Figure 5.2(f).

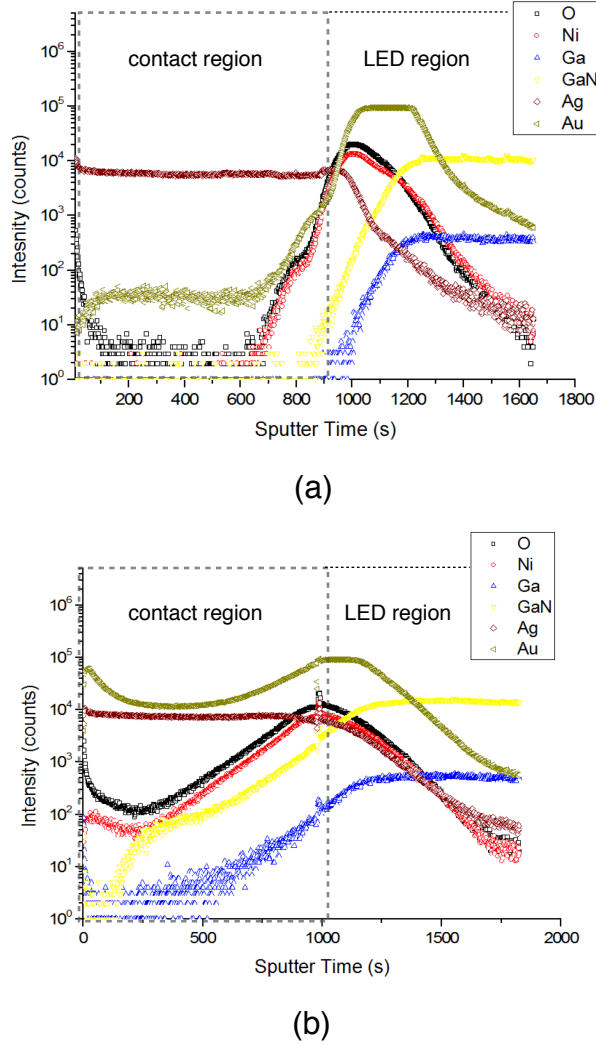


Figure 5.4: The SIMS depth profile of Ni/Au/Ag contact before (a) and after (b) the simulated wafer bonding process.

The SIMS depth profile of Ni/Au/Ag contact before and after the simulated WBP is shown in Figure 5.4. It can be seen that both before and after the WBP, the oxygen profile near the surface of p-GaN layer significantly increased and this profile overlapped the Ni profile. This is an indication of the formation of NiO. It is known that NiO has a work function of 4.9 eV and is a p-type semiconductor [13] forming a p-NiO/p-GaN heterojunction to achieve low contact resistivity. After the simulated WBP, the decrease in the contact resistivity of Ni/Au/Ag can be attributed to Ga out-diffusion. Evidence of this can be clearly seen in Figure

5.4(b), namely the Ga profile broadened into the Ag film, to form most probably a Ag-Ga solid solution. This out-diffusion creates Ga vacancies near the surface of p-GaN layer and Ga vacancies acting as acceptors increasing the net hole concentration near the p-GaN surface, to mitigate band bending and the residual work function difference between p-GaN and the NiO [14].

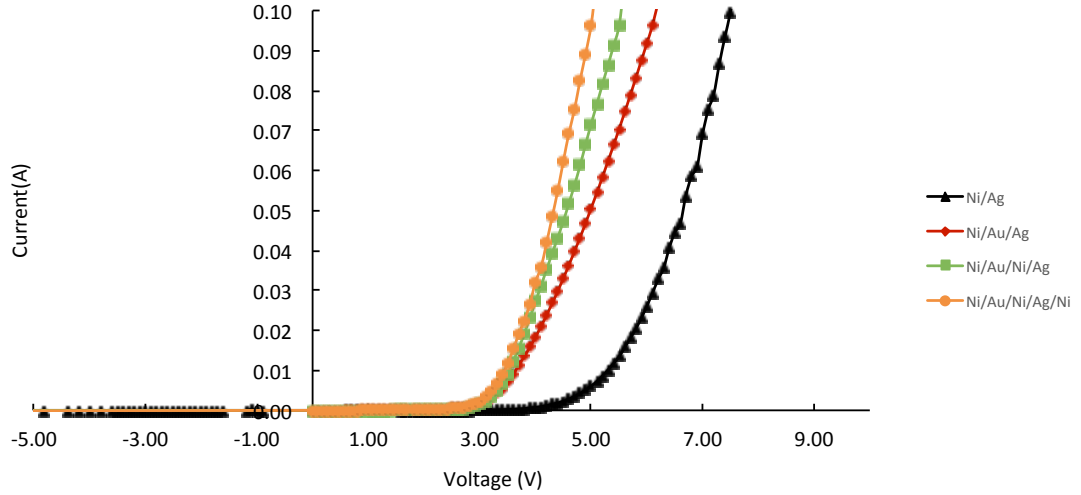


Figure 5.5: *I-V characteristics of the inverted Si-VLEDs with Ni/Ag, Ni/Au/Ag, Ni/Au/Ni/Ag and Ni/Au/Ni/Ag/Ni contacts after the simulated wafer bonding process.*

Figure 5.5 compares the I-V characteristics of Si-VLEDs of 1 mm² device size with the various Ni/Au/Ag-based contacts after undergoing the simulated WBP. It can be seen that the VLEDs fabricated using the Ni/Au/Ni/Ag/Ni, Ni/Au/Ni/Ag and Ni/Au/Ag showed a much better I-V performance, requiring turn-on voltages of only 3.7 V, 3.58 V and 4 V to conduct 20 mA respectively. The relatively high turn-on voltage compared with the state of the art LEDs was due to a voltage drop across an additional resistance contributed by the carrier wafer in the on-wafer probing arrangement. In contrast, the VLED fabricated with the simulated WBP Ni/Ag contact showed a very poor I-V performance, which required 5.7 V forward biased to conduct 20 mA. It is worth noting that the VLED with ITO/Ag contact fabricated by Jeong et. al. [15] required only a turn-on voltage of 3.31 V at 20 mA. Although the turn-on voltage of our VLED with Ni/Au/Ni/Ag/Ni contact is 0.39 V higher than the VLED fabricated by Jeong et. al.. This can be attributed by the Si carrier substrate without any thickness reduction process.

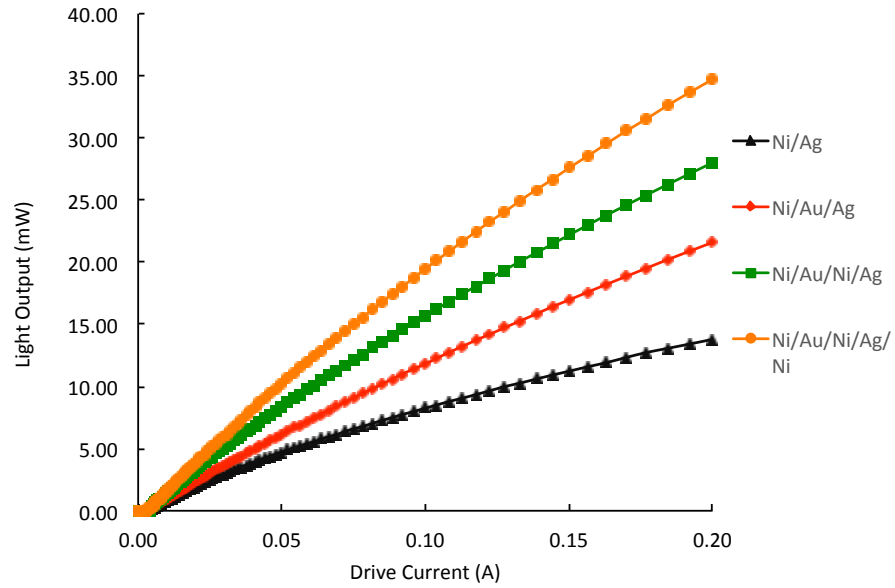


Figure 5.6: The light output power versus LED current measured from the Si-VLEDs with Ni/Ag, Ni/Au/Ag, Ni/Au/Ni/Ag and Ni/Au/Ni/Ag/Ni contacts after the simulated wafer bonding process.

The measured optical power output versus drive current (L-I) characteristics of the VLEDs with the simulated WPB contact structures in Figure 5.6 clearly illustrates the superior properties of the more complex contact structures. It is worth noting that no surface roughening or other strategies were used to enhance light extraction, to enable straight-forward comparison of the resilience of the different mirror p-contact strategies to high temperature WBP. The light output powers at 100 mA drive current for Ni/Ag, Ni/Au/Ag, Ni/Au/Ni/Ag and Ni/Au/Ni/Ag/Ni contacts were 7.5, 10, 15 and 22 mW, respectively. The light output powers at 200 mA drive current were 13, 22, 28 and 35 mW, respectively. It can be seen that the light output performance follows the ranking order of the reflectivity that Ni/Au/Ni/Ag/Ni contact showed the highest light output power and Ni/Au/Ni/Ag showed the second highest. This can be attributed to the insertion of the thin Ni layer underneath the Ag mirror, to prevent Ag agglomeration. This result clearly demonstrates that the VLED fabricated using Ni/Au/Ni/Ag/Ni gave the best light output performance. Although the light output power of our VLED with Ni/Au/Ni/Ag/Ni contact is 6 mW lower than the VLED with ITO/Ag contact fabricated by Jeong et. al. [15], it is still very comparable. It is worth noting that our Ni/Au/Ni/Ag/Ni p-contact not only had gone through a

simulated WBP and also went through an actual 30 minutes wafer bonding process and was still able to produce 22 mW light output power.

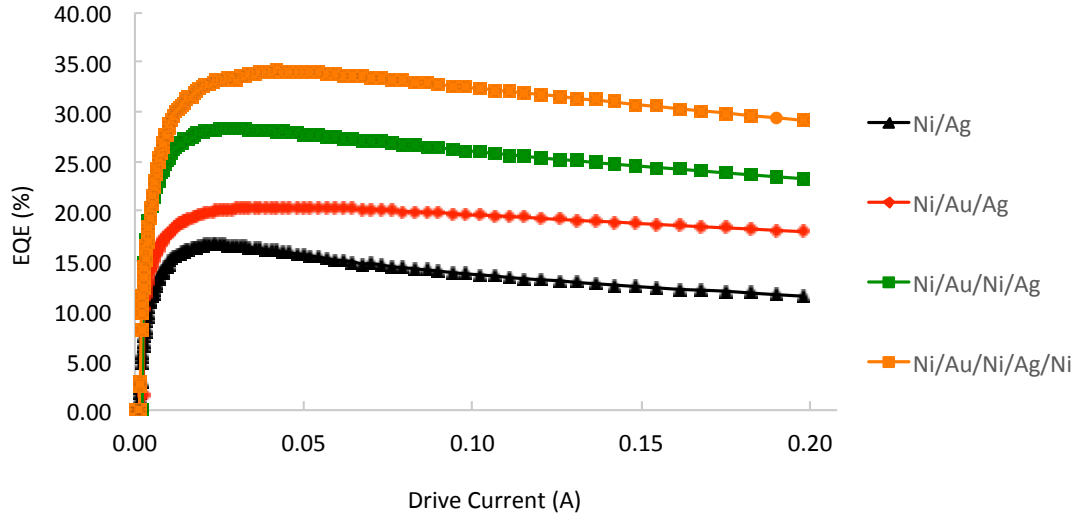


Figure 5.7: The dependence of the external quantum efficiency of the inverted Si-VLEDs with Ni/Ag, Ni/Au/Ag, Ni/Au/Ni/Ag and Ni/Au/Ni/Ag/Ni contacts after the simulated wafer bonding process.

Figure 5.7 illustrates the external quantum efficiency (EQE) of Ni/Au/Ag-based metalized VLEDs after the simulated WBP as a function of drive current. It can be seen that the ranking order of EQE follows that of the L-I performance: namely that the VLED with Ni/Au/Ni/Ag/Ni contact has the highest EQE of 29 % at 200 mA, which is 6 % higher than Ni/Au/Ni/Ag contact and 18 % higher than Ni/Ag. This indicates that inserting Ni(NiO)/Au/Ni TCL underneath the Ag mirror contact with another Ni layer over the Ag can substantially increase the EQE after WBP, despite the lower pre-WBP reflectivity compared to a plain Ni/Ag contact. It is worth noting that VLEDs fabricated using Ni/Au TCL have higher wall-plug efficiencies (WPEs). It can be seen from Figure 5.8 that the VLED fabricated with Ni/Au/Ni/Ag/Ni contact showed 27.2 mW/W of WPE, which is the highest and 19.68 mW/W higher than the VLED fabricated with a simple Ni/Ag reflecting p-type contact.

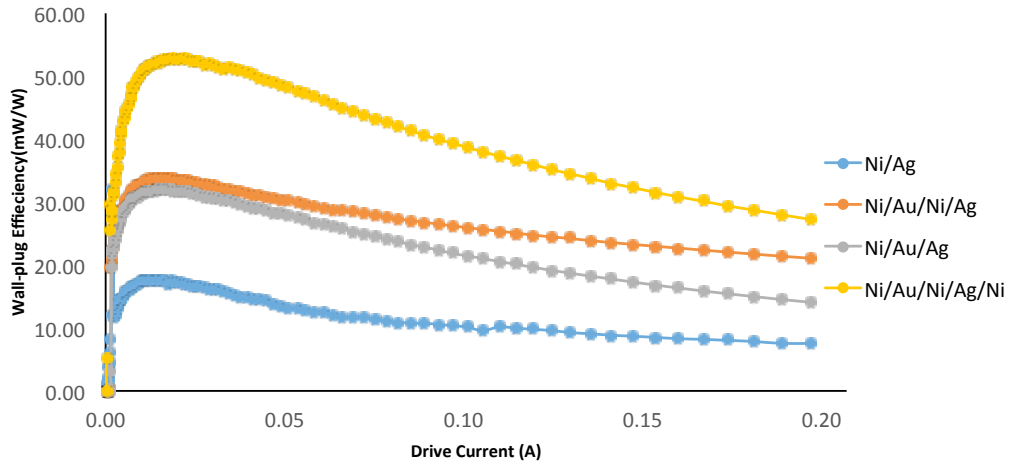


Figure 5.8: The wall-plug efficiency of VLED fabricated with Ni/Ag, Ni/Au/Ag, Ni/Au/Ni/Ag and Ni/Au/Ni/Ag/Ni contacts at 200 mA.

5.4. Conclusion

Procedures for forming a high reflectivity and highly thermally stable ohmic contact for p-GaN layer of InGaN/GaN grown on Si LEDs with inverted vertical structure have been described. The thermal stability of Ni/Au/Ag-based reflective ohmic contacts to p-GaN layer of inverted structure InGaN/GaN vertical light emitting diodes (LEDs) grown on Silicon substrate have been investigated in terms of the electrical and optical properties of finished devices. Before the removal of Si growth substrate and wafer bonding process (WBP) of the InGaN/GaN structure to the Si carrier substrate, the Ni/Ag ohmic contact to p-GaN layer had a very good contact resistivity of $4.79 \times 10^{-4} \Omega\text{cm}^2$ and optical reflectivity of 88 % at 460 nm. In order to study the thermal stability of the contact during the wafer bonding process, the contact was annealed at 450 °C for 30 minutes in air. The Ni/Ag contact after the simulated WBP showed a significant electrical and optical degradation, resulting in an increase of the contact resistivity to $2 \times 10^{-1} \Omega\text{cm}^2$ and a reduction in optical reflectivity to 57 %. However, by inserting Ni/Au transparent contact layers underneath the Ni/Ag contact, the thermal degradation of the contact resistivity was eliminated and the contact resistivity was improved from $3.03 \times 10^{-3} \Omega\text{cm}^2$ of the as-deposited contact to $1.56 \times 10^{-5} \Omega\text{cm}^2$ after the simulated WBP. In addition, the degradation of the optical reflectivity has been mitigated, resulting in only a small decrease from 76 % to 69 %. However, inserting the Ni/Au transparent contact layer

beneath the Ag reflector layer comes at the cost of degrading the starting reflectivity of the contact. The use of thinner Ni/Au layers will mitigate this effect. It is worth noting that although our Ni/Au/Ni/Ag/Ni p-contact produce only 22 mW light output power at 100 mA and required a turn-on voltage of 3.71 V at 20 mA. Comparing these results to VELD with ITO/Ag contact fabricated by Jeong et. al, the light output power and turn-on voltage are 6 mW lower and 0.39 V higher. However, our p-contact is still very comparable. This is because our p-contact not only went through a 30 minute wafer bonding process, but also went through a simulated WBP. Whereas, the VLEDs fabricated by Jeong et. al. only had a 20 minute wafer bonding process.

5.5.References

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Chapter 6

Investigation of the Impact of Carrier Substrate Curvature on VLED Performance

6.1.Introduction

GaN based LEDs are conventionally grown on sapphire substrates and employs $\text{In}_x\text{Ga}_{1-x}\text{N}$ as the active region, in which the emissive colour can be tuned by engineering the quantum well In concentration to achieve green or blue light emission [1]. However, there is a mismatch of lattice constant between the InGaN and GaN interface causing the InGaN multiple quantum well (MQW) to be under compressive stress. This pseudomorphic stress generates a piezoelectric polarization inside the MQW, which changes the shape of the quantum well potential and spatially separates the holes and electrons inside the MQW. This leads impact on the emission wavelength and the internal quantum efficiency [2, 3].

In recent years, the growth of GaN LED epitaxy (GLE) on silicon (Si) substrates by metalorganic vapour phase epitaxy (MOVPE) represents a new technical approach for reducing LED manufacturing costs. Si (111) wafers up to 8 inches are available at a much lower price than sapphire substrates and are compatible with the existing Si processing tools to provide the basis for cost effective device fabrication. Owing to light absorption in the Si substrate, removal and transfer of the GLE on to a carrier substrate with a reflective contact is essential to this technology [4]. This transfer process creates the opportunities not only for inserting a reflective contact to improve the light extraction efficiency, but also causing the stress in the GLE to change without altering the layer structure, as reported by Xiong et al [4] and Chen et al [5].

There have been reports on the reduction of quantum confined stark effect (QCSE) in the GLE grown on sapphire substrates transferred to Si substrate by using laser lift-off technique [5, 6]. However, there is disagreement in the reports of the effect of transferring GLE grown on Si to a carrier substrate. Xiong et al found that a red-shift in the MQW emission wavelength resulting from decreased in-plane tensile stress in the GLE after the transfer to a Si carrier substrate process caused an increase in the compressive stress in the MQW. On the other hand, Chen et al, measured a 5 nm blue shift attributed to a partial tensile strain relaxation after the GLE was transferred from the Si substrate to a copper submount. In both cases, the MQW emission wavelength of the lateral LEDs remained within a 450-445 nm. The composition difference in the InGaN layers of MQW was minimal in these works.

Exploiting these differences in behaviour and the scope to improve the internal quantum efficiency (IQE) of LEDs by post-growth stress engineering requires a more detailed investigation of the layer by layer stress variation in the heterstructure and of the wafer bonding induced stress. This chapter reports such a study to reveal how the GLE transfer process allows the stress in GaN to change to reduce QCSE without altering the layer structure during the growth process by designing an optimal bonding stress-induced curvature of the GLE via careful selection of the Si carrier thickness. High resolution x-ray diffraction (HR-XRD), photoluminescence (PL) measurements and dynamic photoluminescence (DPL) were employed to study the strain induced optical changes of the MQW.

6.2.Quantum Confined-Stark Effect

III-Nitrides are conventionally grown on a sapphire or SiC substrate cut in the [0001] direction [7]. The atoms in III-Nitride semiconductors are structured in closely spaced hexagonal bilayers along this direction. One layer is made up entirely of cations (In, Ga atoms) and the other layer is made up entirely of anions (N atoms). The different electronegativity of N and Ga (or In) atoms causes a polarity difference between these two layers, which sets up an internal electric field inside the material called spontaneous polarization (P_{sp}). Fortunately, the spontaneous polarizations that InGaN/GaN LEDs experience

are very small as there is only a small polarization constant mismatch between GaN (-0.029 Cm^{-2}) and InN (-0.032 Cm^{-2}) materials [8].

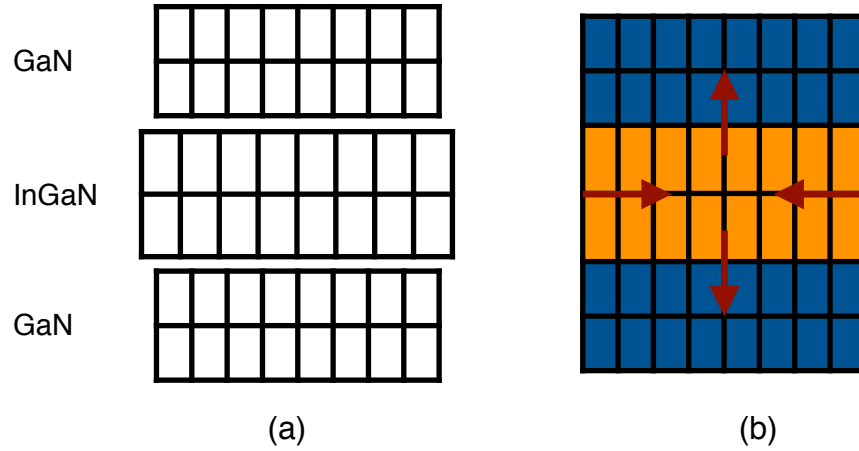


Figure 6.1: InGaN grown between GaN barriers in [0001] direction experiences compressive strain, where (a) the illustration in lattice format and (b) when the epitaxy layers are put together.

However, the spontaneous polarization is not the only polarization effect that can be found in III-Nitrides. The wurzite III-Nitrides also possess the property of piezoelectric polarization property as they do not have centres of symmetry. This means that a strain induced polarization is also produced when the material is strained. The direction of this piezoelectric polarization field (P_{pz}) is determined by whether or not the material is under tensile or compressive stress. A strain can be induced when there is a lattice constant mismatch between two layers in a heterostructure. As mentioned, blue and green GaN based LEDs employ $\text{In}_x\text{Ga}_{1-x}\text{N}$ quantum wells as the active region, in which the colour emitted by LEDs can be tuned by adjusting the In concentration in the quantum well (typically an In mole fraction of 15 percent for blue colour and 21 percent of In for green colour) [2]. However, InGaN layer has larger lattice constant than the GaN layer and the thermal expansion of sapphire is larger than that of GaN. As a result, the quantum well is under large compressive strain as illustrated in Figure 6.1(b). This compressive strain induces a large piezoelectric polarization field inside the quantum well. As a consequence, the shape of the quantum well potential is changed by the net polarization as illustrated in Figure 6.2(a), leading to the reduction of effective band gap energy of the quantum well, which causes the peak wavelength emitted by the LED to be red-shifted. In addition, this large piezoelectric field also causes the electrons

and holes inside the quantum well to be spatially separated, which reduces the overlap of electron and hole wave functions. As a result, the radiative recombination rate is reduced, leading to a lower internal quantum efficiency. This phenomenon is known as the Quantum Confined Stark Effect (QCSE) [2].

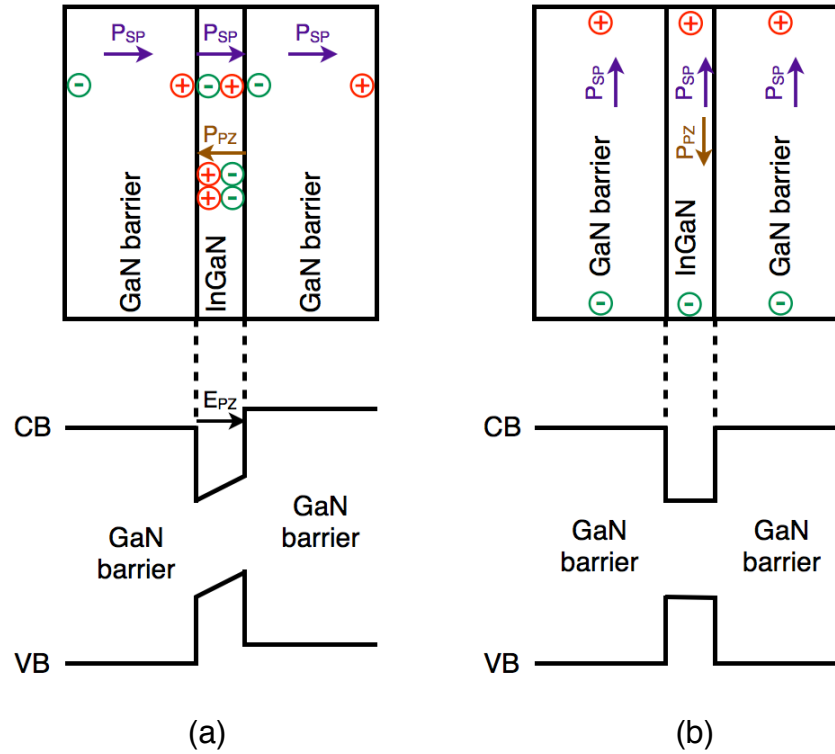


Figure 6.2: Schematics of (a) a quantum well potential is deformed by QCSE (b) a quantum well without the presence of QCSE [inspired by 9].

One possible way to solve QCSE problem is to grow III-Nitrides in non-polar directions such as $[1\bar{1}00]$ or $[11\bar{2}0]$. Figure 6.2(b) shows the potential profiles of quantum wells grown on $[11\bar{2}0]$ planes, where the piezoelectric polarisation does not influence the quantum well potential profile. Figure 6.3 illustrates the positions of hexagonal crystal structure a) in $[0001]$ direction and b) in $[1\bar{1}00]$ and $[11\bar{2}0]$ directions. However, III-Nitrides grown in these directions suffer from a high density of stacking faults, which give rise to spectral broadening of the quantum well luminescence [10]. Furthermore, $[11\bar{2}0]$ sapphire or Si substrates are expensive in 6-inch diameter. As a consequence, it is still strongly favoured to grow the GaN epitaxy on c-plane sapphire and Si (111).

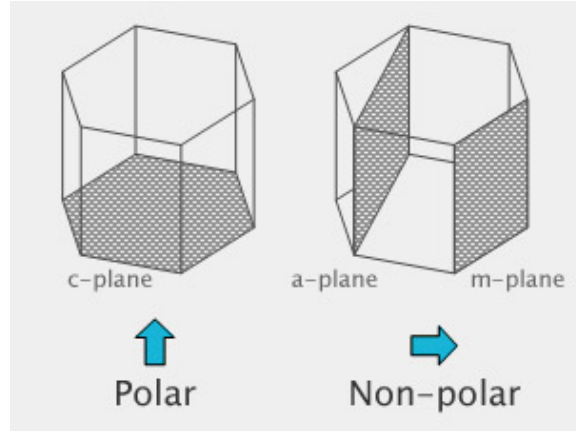


Figure 6.3: Schematics of a) the position of $[0001]$ direction and b) $[1\bar{1}00]$ or $[11\bar{2}0]$ directions on the hexagonal crystal structure [9].

6.3.Experimental Details

An as-grown InGaN/GaN LED wafer grown on a 150 mm diameter Si (111) substrate was supplied by Plessey Semiconductor plc, and PL measurements revealed the wafer is highly uniform as no noticeable variations in the peak wavelength of the MQW were observed across the wafer. This wafer has a 650 nm AlGaIn buffer layer with composition of followed by 1470 nm n-GaN, 200 nm thick InGaIn/GaN multiple quantum wells (MQWs) and 95 nm of p-GaN. The centre part of wafer was cleaved into 1cm^2 square fragments for convenience and then used in different bonding processes. Next, the epitaxy was pixelated into $\sim 1\text{mm} \times 1\text{mm}$ mesa structures by ICP etching (Cl_2/Ar) through the p-GaN layer and MQWs into the n-GaN and back-filling the trench with SiO_2 deposition by plasma enhanced chemical vapour deposition (PECVD). Ni/Ag/Ni (1 nm/200 nm/10 nm) multi-metal layers were first deposited by E-Beam evaporation on to p-GaN mesas to form a highly reflective p-GaN ohmic contact, followed by rapid thermal annealing at 450°C in oxygen environment for 2 min to form a good ohmic contact. multilayer bonding metals of Ni ($0.1\ \mu\text{m}$), Sn ($1.7\ \mu\text{m}$) and Ag ($3.5\ \mu\text{m}$) were then deposited by E-Beam evaporator on to this p-type contact, as well as the Si carrier wafer for wafer bonding process. These layers have larger thermal expansion coefficients (Sn: $1.4 \times 10^{-5}\ \text{K}^{-1}$; Ag: $1.9 \times 10^{-5}\ \text{K}^{-1}$), as well as a combined greater total thickness than the Nitride layers. The LED wafer was then put in contact with a $475\ \mu\text{m}$ or $675\ \mu\text{m}$ thick Si carrier substrate under nitrogen at a pressure of 6 MPa in a purpose-built wafer bonder to realise bonding at 260°C for 30 minutes. Then, the Si growth substrate was removed

by a combination of mechanical lapping and inductively coupled plasma (ICP) etching with SF_6 plasma. Finally, the nucleation layer of AlN and the AlGaN alloy grading layer were plasma-etched away to expose the Nitrogen face (N-face) n-GaN for the deposition of multi-metal n-type ohmic contact, which comprised of Ti/Al/Ni/Au (20 nm/200 nm/20 nm/100 nm)

To understand the local stress states in different GaN layers before and after the growth substrate removal, the room temperature dynamic photoluminescence (DPL) measurement technique described in ref. 11 was performed using a Renishaw InVia Raman microscope with a CW He-Cd 325nm laser in conjunction with stress state measurements determined from HR- XRD 2θ - ω GaN (0002) scans obtained with a Bede D1 diffractometer. The substrate curvature measurements were performed using a Detak surface profiler before and after removing the Si growth substrate. PL emission spectra of the MQW were measured at room temperature with a Andor Spectrometer using a 405 nm blue diode laser for excitation to ensure only the MQW was excited. The light output-current-voltage characteristics of the VLEDs were measured under 10ms pulsed conditions on a 1s duty cycle (to minimize self-heating) on-wafer using a current-voltage source unit (Keithley 2600) with an integrating sphere instrument placed 3mm above the wafer surface over low-profile electrical probes.

6.4. Results and Discussions

6.4.1. Reversal of Stress-Induced Chip Curvature

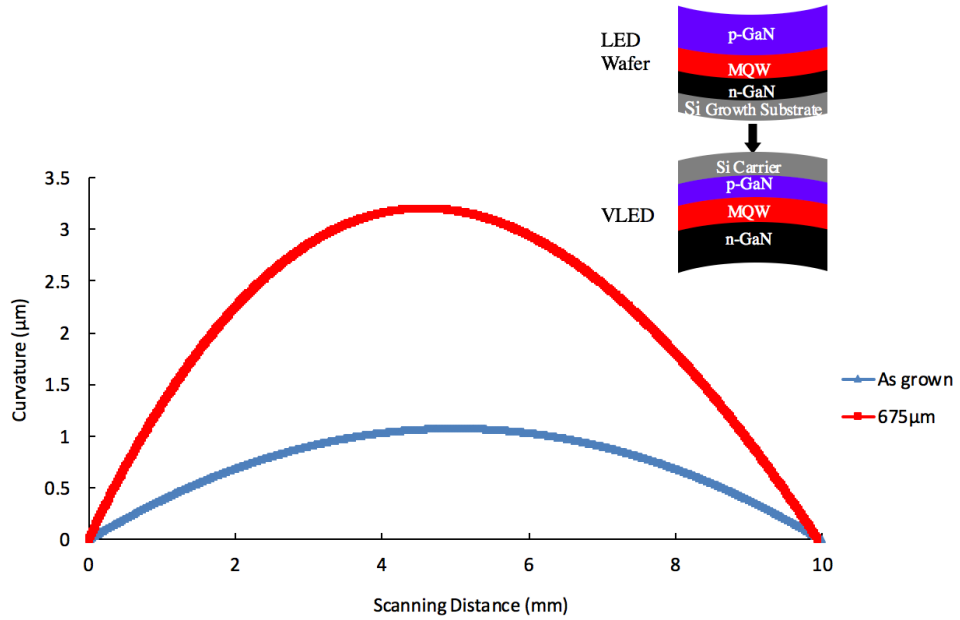


Figure 6.4: The curvature profile of the backside of Si growth and carrier substrates.

Figure 6.4 illustrates the radius of curvature of an as-grown LED sample and a processed GaN VLED samples bonded on a 675 μm thick Si carrier substrate measured from the back of the Si growth substrate and Si carrier substrate respectively. Note that the GLE undergoes a change from concave to convex curvature, hereafter called curvature flip as shown in the inset of Figure 6.4. The curvature is a consequence of Si having a smaller coefficient of thermal expansion (CTE) than GaN and the bonding metals. Both: will shrink more than the Si growth substrate resulting a stress gradient in the LED epitaxy during the cool down step in the growth process [12]. The curvature result measured from the backside of the as-grown sample showed a concave curvature of $\sim 1.2 \mu\text{m}$ per cm, which is an evidence of the pre-existing stress gradient in the GaN in which the inner surface of the bowed composite structure will be under compressive stress [12]. When the LED epitaxy was bonded to a 675 μm thick Si carrier substrate with the original growth substrate removed, the GLE becomes bowed in the opposite direction the free inner surface now being the top (previously bottom) of the AlGaIn alloy grading layer, showing a curvature of

$\sim 3.2 \mu\text{m}/\text{cm}$. This result demonstrates there has been a change in the stress of the structure on wafer bonding and growth substrate removal.

The reason of the resultant n-side up LED structure was found to change from a concave to a convex curvature, as illustrated in the inset of Figure 6.4 is, as mentioned in the experimental method section, because transfer of the GLE to a Si carrier substrate involves a thermal treatment and the addition of metal layers of both radically different CTE and of total comparable thickness to the GaN-based epitaxy. These properties combine to induce an additional stress to the LED epitaxy. In the as-grown structure, the Si structure is under compressive stress due to the higher CTE of the GaN-based LED epitaxy. A similar compressive stress occurs in the Si carrier substrate after cool down from the wafer bonding. When the original Si growth substrate is removed, the part of the LED epitaxy adjacent to the free surface is able to bow reducing its tensile stress, while the bonding metal still exerts compressive stress on the Si carrier substrate. As a result of both these effects, the Si carrier will curve towards the bonding metal causing the observed curvature flip of the LED layers.

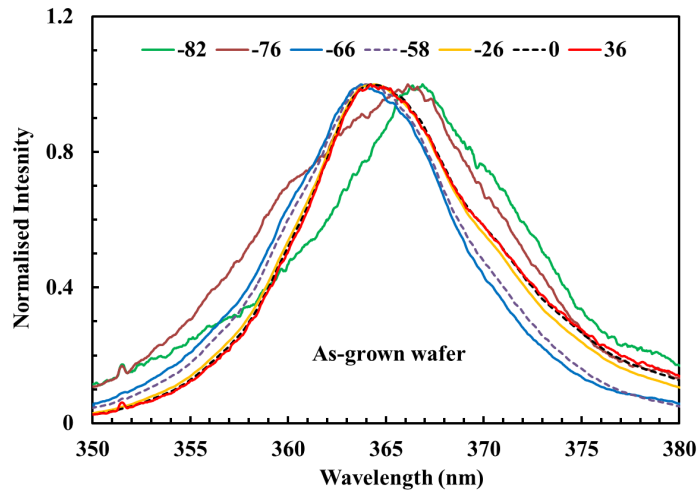
Sample bowing implies there is a stress variation across a multilayer structure: the material closest to the inner radius will be under compressive stress, or less tensile stress, while the material closest to the outer radius will be under more tensile stress [11]. Since the MQW is almost always offset from the middle of the GLE, the curvature flip means that the average stress in the emissive region will change on wafer bonding. This will affect the emitted wavelength via the QCSE.

It is obvious that the original tensile stress in the GLE has played an important role in initiating the curvature flip. The effect of the bonding temperature, the material and thickness of the bonding metal layers must also be taken into account. The bonding layer, which had a total thickness of $\sim 6 \mu\text{m}$ also applies compressive stress to the Si carrier and strongly by influences the final curvature. Since Ag comprises about 67 % of the total thickness of the bonding layer, the combined contribution to the stress of the metal layers may be estimated via [12]

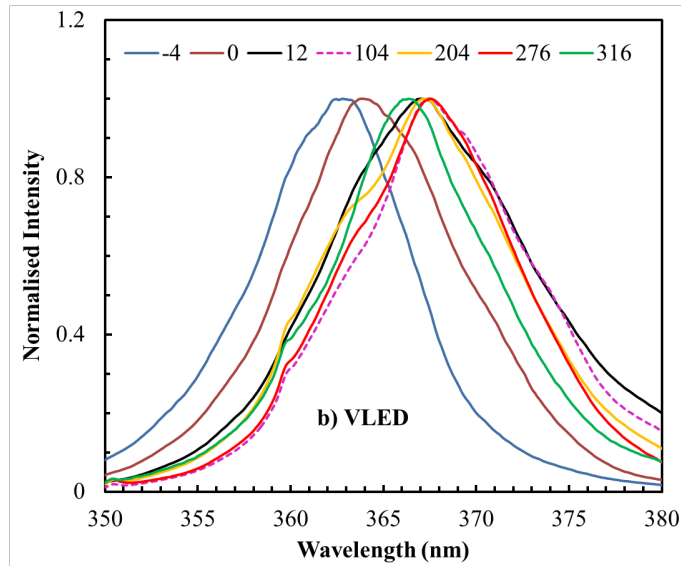
$$\sigma \approx \left(\frac{\alpha_{Ag} - \alpha_{Si}}{1 - \nu} \right) E \Delta T \quad (6.1)$$

where $\alpha_{Ag} = 18.9 \times 10^{-6} \text{ K}^{-1}$ and $\alpha_{Si} = 3 \times 10^{-6} \text{ K}^{-1}$ are CTEs of Ag and Si, respectively [12]. ΔT is the difference between the wafer bonding temperature and room temperature. The ν is in equation (6.1) the poisson's ratio of Ag and E is the Young's modulus of Ag. Using these values in equation (6.1) and a wafer bonding temperature of 260 °C, an estimated compressive stress of ~0.5 GPa is exerted on the Si carrier substrate after cool down from the process of wafer bonding. Average stress in a similar estimate of the LED epitaxy is not possible because of the pixelation into device mesas and effect of dislocations in the epitaxy both introduce a depth dependent relief of the strain.

6.4.2. Stress Characterisation



(a)



(b)

Figure 6.5: The Cross-sectional variation of the peak position of the room temperature GaN band edge PL spectra of (a) before bonding GaN LED wafer and (b) processed GaN VLED wafer with its original growth Si substrate removed.

In order to study the stress change during the curvature flip, a cross-sectional PL measurement described in section 3.5 was performed. Figure 6.5(a) shows the cross-sectional DPL spectra of the as-grown wafer. These were obtained by moving a laser beam (effective diameter: $\sim 200 \mu\text{m}$) from above and parallel to the plane of the upper p-GaN surface towards the Si growth substrate in steps of $2 \mu\text{m}$. Note, the DPL technique relies on moving the sample through the edge of a Gaussian-shape laser beam where the intensity gradient is maximum, with

the effect that by the relative positions at which the PL spectra are measured can be determined with respect to a selectable origin. In Figure 6.5 these estimated positions are super-imposed on the GLE, with the numbers above each point indicating their measured position with respect to the origin. The method of selecting the origin is described below. Figure 6.5(b) shows similar cross-sectional PL spectra obtained from the wafer bonded VLED sample by moving the same laser beam (effective diameter: $\sim 200 \mu\text{m}$) from above and parallel to the now uppermost n-GaN towards the bonded Si carrier substrate in steps of $4 \mu\text{m}$. An increase in laser step size was required to travel the thicker n-GaN buffer layer of the epitaxial structure. With a circular laser beam shape and a Gaussian beam profile, the recorded PL spectra may change with laser beam positions should there be a variation with depth in the stress in the multilayer structure, as described in Ref. 11. The effective laser beam diameter is defined as the distance the laser beam moves from where a GaN PL signal was first detected above the noise level to where the GaN band edge PL signal again drops to the level of noise. The legends names above each point in Figure 6.5 corresponds to the laser beam positions in μm and legend 0 corresponds to where the centre of the laser beam overlapped the surface of the LED epitaxy. So, the values increase from negative to positive as the laser beam moves from the LED epitaxy towards the Si substrate. For clarity, not every distinctive spectrum is plotted in Figure 6.5(a) & 6.5(b), merely those that reveal critical changes in the strain profile. It can be seen from Figure 6.5(a) that the peaks of the PL spectra undergo a small blue shift from the wavelength of 366.8 nm to 363.7 nm (i.e. blue shifted) as the laser beam position moves from the p-GaN/top part of the LED epitaxy layer towards the Si growth substrate. This indicates that the GLE near the MQW experiences a higher tensile stress, owing to the higher dislocation density in the n-GaN layer close to the AlN layer, where stress is relieved via the formation of threading dislocations. The dislocation density is reduced as the n-GaN layer thickness is increased, with the effect that stress builds up near the MQW [2]. For the processed GaN VLED wafer, the recorded PL spectra are red-shifted towards the p-GaN to reveal shows a similar stress distribution as in the as-grown sample (Figure 6.5(a)) when the laser is scanned from the free surface of the LED epitaxy to the Si carrier substrate. However, the red-shift range is much larger (from $\sim 362.8 \text{ nm}$ to $\sim 367.8 \text{ nm}$). This corresponds to an increase in tensile stress in the LED

epitaxy causing the wavelength of GaN PL to be red-shifted. The curvature flip also causes the relatively low tensile-strained LED epitaxy, which is close to the AlN nucleation layer, to undergo a further reduction in tensile stress compared to the relatively highly tensile strained LED epitaxy close to MQW, which experiences an increase in tensile stress. This interpretation is consistent with HR-XRD spectra of the ω - 2θ GaN (0002) scan curves as shown in Figure 6.6, where that of GaN VLED is slightly broadened, i.e. increased x-ray photon counts at both larger and smaller 2θ angles than average. In addition, from the HR-XRD results, the top shoulder of the x-ray intensity of the bonded VLED samples in the $\Delta 2\theta > 0^\circ$ region is increased whilst that of $\Delta 2\theta < 0^\circ$ region is decreased. According to Bragg's law, $\theta = \arcsin(n\lambda/2d)$, an increase in the 2θ indicates that the c-lattice constant becomes smaller, which implies that the tensile stress in the bottom part of the GLE of the bonded VLED is increased whilst the tensile stress in the top part of the LED epitaxy is decreased.

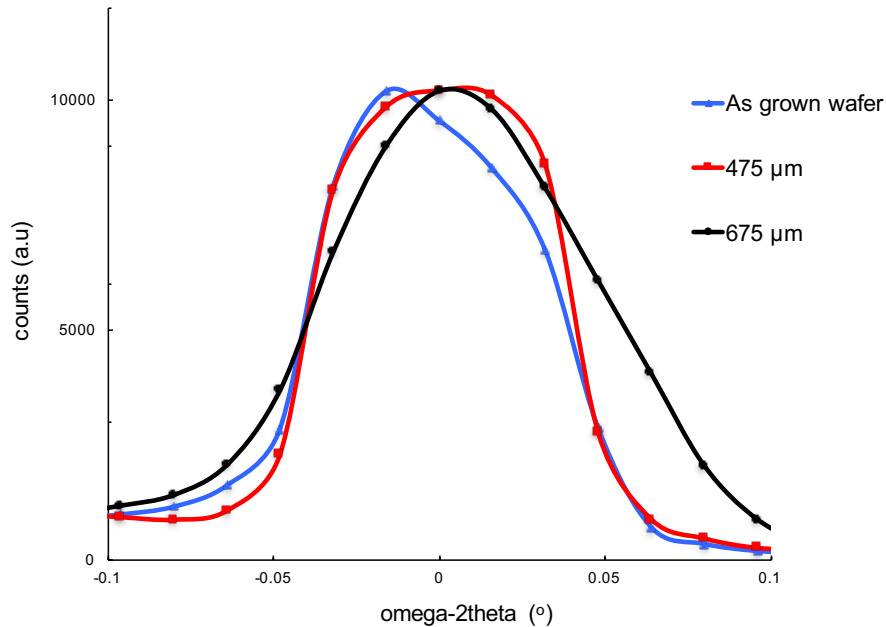


Figure 6.6: ω - 2θ scan curves of unprocessed LED epitaxy and fully processed VLED bonded on to 475 μm and 675 μm .

It is well known that the wavenumber of the $E_{2(\text{high})}$ mode of the Raman scattering spectrum of GaN provides a sensitive measure of strain in the layer structure [6], [11]. The $E_{2(\text{high})}$ of peak in the as-grown LED structure occurs at 563.7 cm^{-1} indicating the epitaxy is under a high volume-averaged tensile stress [14]. The Raman spectroscopy showed a similar behaviour as the XRD measurements. Figure 6.7 compares the Raman spectra of the unprocessed

LED wafer and processed LED wafers, where the spectra of both processed GaN VLEDs bonded to a 475 μm thick or a 675 μm thick Si substrate are slightly broadened, indicating that the variation of stress across the whole layer structure is greater in agreement with the DPL measurements. The lower wavenumber region of the Raman signal intensity curves for both the processed VLED samples bonded onto 475 μm and 675 μm (i.e. $564\text{ cm}^{-1} < \text{wavenumber}$ for low wavenumber region and $565\text{ cm}^{-1} > \text{wavenumber}$ region for high wavenumber region) is increased whilst the intensity of the high wavenumber region is decreased in the ~ 560 to 565 cm^{-1} wavenumber range. This result indicates that the presence of layers of increased tensile stress, which is in agreement of the DPL results which revealed that the tensile stress in the GLE of near the bonding metal is increased and near the free surface of the GLE is decreased. In addition, the Raman peak of the LED epitaxy bonded onto 675 μm carrier substrate was red shifted to 565.5 cm^{-1} from 563.71 cm^{-1} , which can be attributed to the shrinkage of the n-GaN layer back towards an unstrained state at the inner radius free surface of the bowed structure where the Stoney's theory states the composite structure will be under compressive stress. However, when the LED epitaxy was bonded on to a thinner substrate (i.e. 475 μm), the Raman peak shift was much smaller: from 563.71 cm^{-1} to 563.74 cm^{-1} . This correlates with a larger measured Si carrier substrate curvature, which stretches the LED epitaxy, leading to an increase in the tensile stress in the bottom part of the GLE of the VLED close to the bond whilst the GaN layer adjacent to the free surface of the GLE at the inner surface of the bowed structure will be under increased compressive stress (i.e. less net tensile stress).

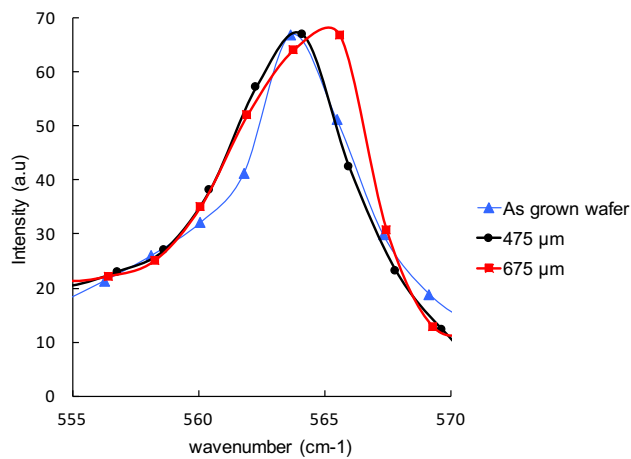


Figure 6.7: The Raman spectroscopy of VLED bonded on to 675 μm and 475 μm .

6.4.3. Impact of Substrate Thickness

Figure 6.8 compares the curvature measurement as a function of scanning distance for the as-grown sample with that of the GaN VLED samples bonded on Si carrier substrates with the thickness of 475 μm and 675 μm . The curvature results of the processed GaN VLED samples were measured to have a convex bow from the backside of the Si carrier substrate, relative to the concave curvature of the as-grown LED sample. In other words, the resultant n-side up LED structure was changed from a concave to a convex curvature. As mentioned in the experimental method section, this occurs because transferring the LED epitaxy to a Si carrier substrate is carried out at an elevated temperature, which induces an additional tensile stress to the LED epitaxy and compressive stress in both Si carrier and growth substrates during the cool down step via the greater contraction of the metal bonding layers. When the p-GaN surface is bonded to a carrier substrate and the original Si growth substrate is removed, the n-GaN layer becomes the top part of LED and is therefore no longer clamped, so can further partially relax from its previous tensile stress state, with the bonding metal exerting additional compressive stress on the Si carrier substrate. As a result, the Si carrier now bows up towards the bonding metal causing a curvature flip of the whole structure (see inset of Figure 6.4). This can also be seen from the DPL results of the as-grown wafer, which show that the stress distribution across the LED epitaxy is not uniform; notably that the top the LED epitaxy (i.e. the p-GaN) of the as-grown wafer is under larger tensile stress compared with the bottom of the GLE (i.e. the n-GaN). However, as seen in Figure 6.5(b) when it is bonded to a Si carrier with the original Si growth substrate removed, a greater spread in the GaN band edge luminescence is observed as the laser beam moves from the top n-GaN layer towards the Si carrier substrate. This confirms that the n-GaN of the processed GaN VLED sample has a smaller tensile stress than the same layer had in the as-grown sample due to the relaxation of tensile stress on removal of the Si growth substrate, whilst the p-GaN of the wafer bonded sample has a larger tensile stress than the p-GaN of the as-grown sample due to the curvature flip. The extent of the reversal of curvature depends on the carrier substrate thickness. A thinner carrier substrate is less stiff and therefore will bow more. As it can be seen in Figure 6.8, where the bow for wafer bonded

structures with 675 μm and 475 μm Si carrier substrates, has measured of curvature of $\sim 3.2 \mu\text{m}/\text{cm}$ and $\sim 6 \mu\text{m}/\text{cm}$ curvatures respectively.

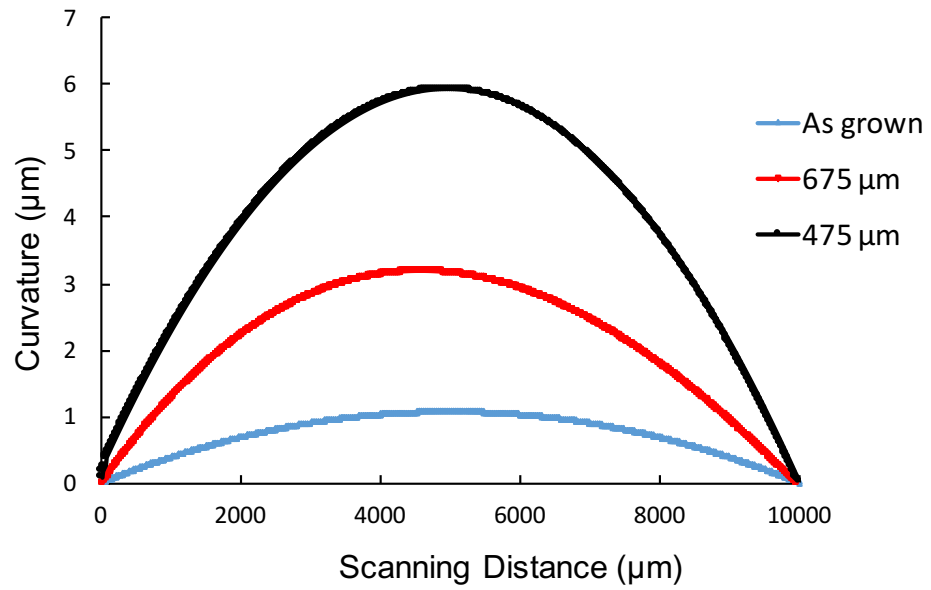
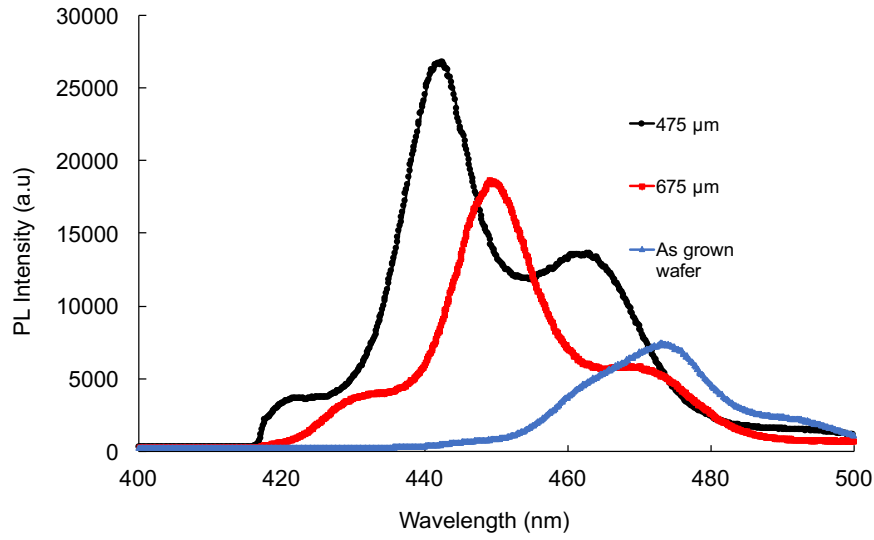
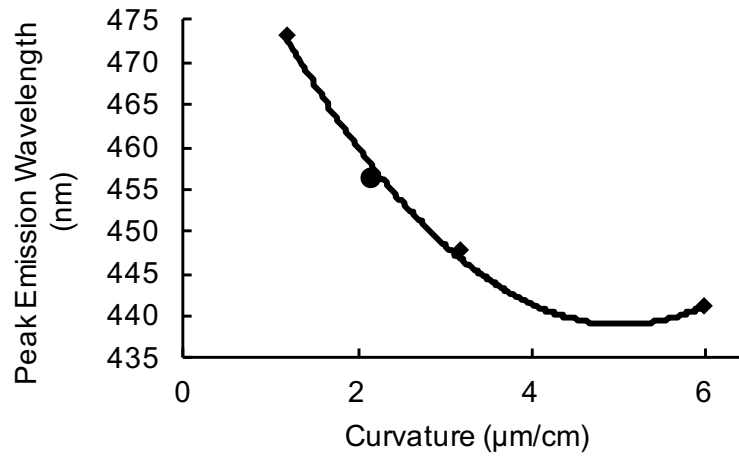


Figure 6.8: The curvature profile of the backside of Si growth and carrier substrate with 675 μm and 475 μm .

6.4.4. Light Output Characterization



(a)



(b)

Figure 6.9: (a) Comparison of the room temperature MQW PL of the two GaN/InGaN LED structures wafer-bonded onto 475 or 675 μm thick Si carrier substrates with that of the as-grown epitaxy structure. (b) Variation in emission peak wavelength with sample curvature; square points: LED epitaxy as grown or wafer-bonded onto 475 or 675 μm thick Si carrier; solid circle: fully processed thinned VLED on 675 μm thick Si; black line: quadratic fit to the four data points shown.

Figure 6.9(a) compares the MQW PL spectra of the as-grown unprocessed LED epitaxy and the fully processed GaN VLEDs for the two Si carrier wafer thicknesses. It can be seen that the MQW PL spectrum of the as-grown sample peaks at 470 nm, corresponding to a quantum well transition energy of 2.638 eV. Once the GLE was transferred to the replacement substrate, the MQW PL

peak of the processed GaN VLED bonded on 675 μm thick Si carrier blue-shifts to 448 nm, corresponding to an increase in quantum well transition energy of 130 meV. This can be attributed to the reversal of curvature, which has the effect of stretching the GLE to counteract the compressive, pseudomorphic stress in the InGaN layers of the MQW and thus reduce the piezoelectric contribution to the net polarization and, with it, the QCSE induced red-shift in the MQW emission. An increase of band gap energy of 180 meV can be achieved by using thinner Si carrier substrate of 475 μm , this is because a thinner substrate is less stiff and a larger curvature flip is obtained.

The reduced QCSE contributes to the observed ~ 3.3 fold increase in the PL intensity, of which at most only a factor ~ 2 can be attributed to replacing the light absorbing Si substrate with a reflecting p-type contact and to the slight increase in nano-scale roughness that occurs on substrate removal. Figure 6.9(b) shows the variation in emission peak wavelength with sample curvature for the LED epitaxy as grown or wafer-bonded onto the 475 or 675 μm thick Si carrier wafer. The solid black line is a quadratic fit to the four data points, chosen because of the expected quadratic dependence of the QCSE on polarization (electric field) [15], [16]. The flattening of the quadratic fit for emission wavelengths near 450 nm indicates the tensile stress introduced by wafer bonding onto the 475 μm thick Si carrier almost cancels out the pseudomorphic stress in the MQW and is therefore close to optimum since the QCSE is negligible. The solid circle in Figure 6.9(b) shows the effect on wafer bow and peak emission wavelength of removing 500 nm of the LED epitaxy (the AlN/AlGaIn strain management layers and the unintentionally doped GaN buffer layer) by Cl_2/Ar ICP etching the wafer bonded onto a 675 μm thick Si replacement substrate.

The fact this datum lies on the same quadratic trend line reveals that the additional stress in the LED epitaxy induced by the wafer bonding process complies qualitatively with the Stoney's theory [17]. However, as stated above, the presence of dislocations in the AlGaIn/GaN/InGaIn heteroepitaxy and their impact on the pseudomorphic strain, plus the effect of ICP etching of the LED structure to form device mesas prior to wafer bonding inhibit a simple quantitative analysis. On the other hand, as the data in Figure 6.9(b) shows,

optimization of the strain profile in the MQW after wafer bonding can be achieved empirically by thinning the LED epitaxy or by post-bonding thinning the replacement substrate. Other options include changing the thickness of the bonding metals used, the bonding temperature or even adopting a different solder.

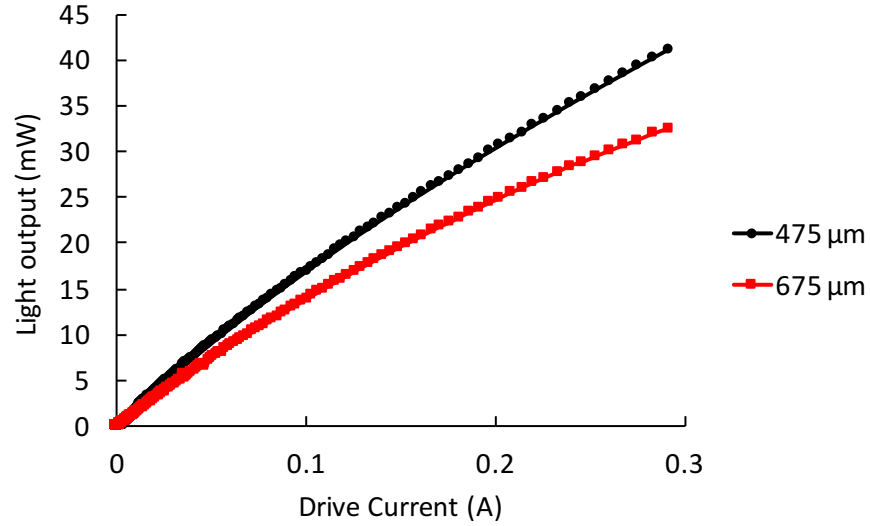


Figure 6.10: The light output characteristics of VLED bonded on 675 μm and 475 μm Si carrier substrates.

Figure 6.10 illustrates the measured light output power of unroughened 1 mm² GaN VLEDs bonded on Si carrier substrates with thickness of 675 μm and 475 μm as a function of drive current. It can be seen that the GaN VLED bonded on to a thinner Si substrate has ~25 % higher light output power of 41 mW at the drive current of 300 mA, which is 8 mW higher than that of the GaN VLED with thicker Si carrier substrate. Although both GaN VLEDs have the same device structure and mirror contact material, the measured light output powers of LED epitaxy bonded to 675 μm Si carrier substrate showed a weaker light output, which can be attributed to the smaller reduction of QCSE via curvature flip compared with devices bonded to the 475 μm carrier substrate.

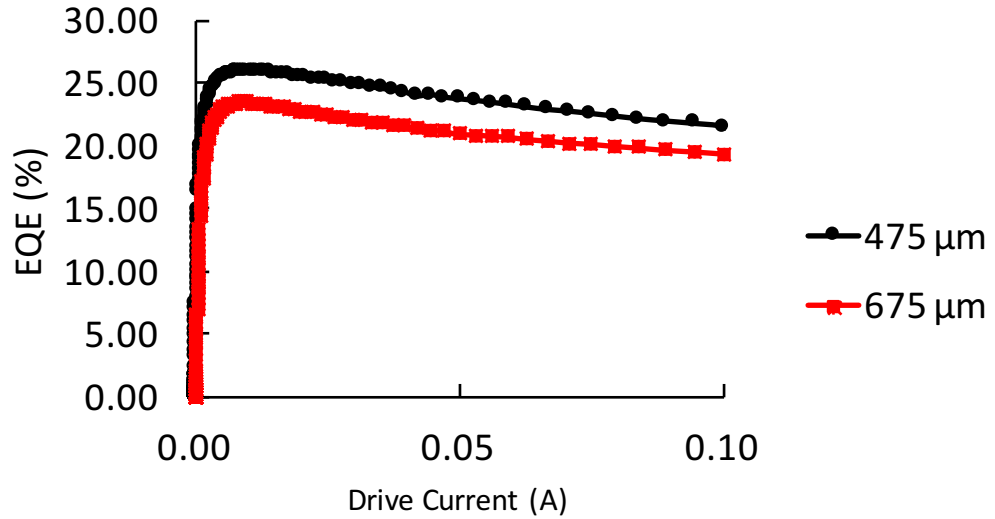


Figure 6.11: The EQE of GaN VLED bonded on to 675 μm and 475 μm Si carrier substrates.

Figure 6.11 shows that the external quantum efficiency (EQE) of GaN VLEDs bonded on to Si carrier substrates as a function of drive current calculated from the data in Figure 6.10. The VLED bonded on to a thinner Si substrate showed an EQE of 23 % at the drive current of 300 mA, which is 4 % higher than that of the VLED with 675 μm Si substrate. This result indicates that the EQE can be improved by management of the net stress in the MQW, in this case by bonding the GLE on to a thinner thickness of Si carrier substrate without altering the GaN growth layer structure or the wafer bonding process.

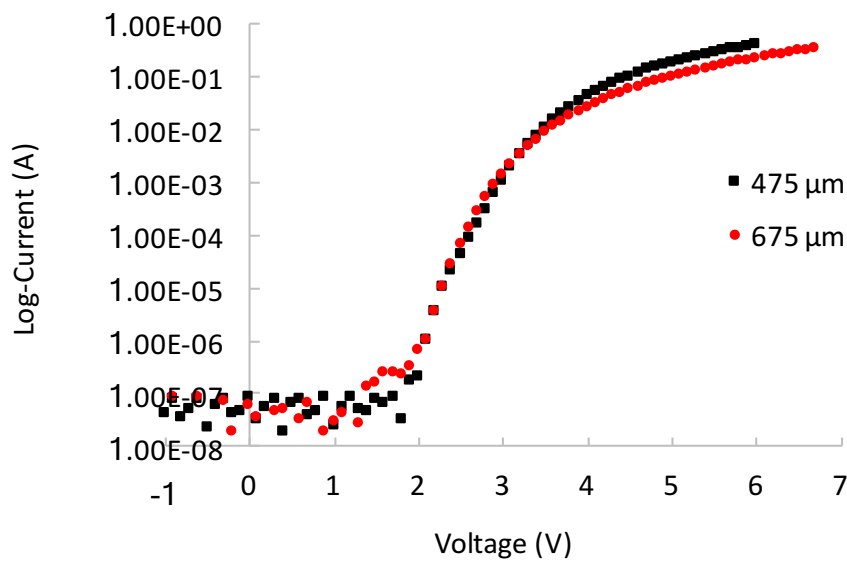


Figure 6.12: The I-V characteristics of GaN VLED bonded to 675 μm and 475 μm Si carrier substrates.

Figure 6.12 shows the current-voltage (I-V) characteristics of GaN VLEDs bonded on to two different thickness of Si carrier substrates. It can be seen that although both GaN VLEDs had the same device structure, they still showed a different operational voltage at the drive current of 300 mA. The GaN VLEDs with a 675 μm and 475 μm thick Si carrier substrates showed an operational voltages of 6.7 V and 5.7 V at 300 mA respectively. The reduction of operational voltage for the thinner Si carrier substrate can be attributed to lower series resistance contributed by the thinner Si substrate. This result indicates that by using a thin Si substrate not only reduces the QCSE, leading to an increase in the EQE, but also allows greater freedom in designing chip layouts that minimise wall plug efficiency reducing series resistance.

6.5.Conclusion

This work presented in this chapter has shown that the compressive due to the pseudomorphic epitaxial growth of InGaN and GaN stress in the MQW grown on Si (111) substrate can be partially relaxed without altering the GLE layer structure to reduce the QCSE by appropriate design of the wafer bonding process. By transferring the GLE to a Si carrier substrate and removing the original Si growth substrate, a reversal of GLE curvature is obtained by relaxation of tensile strain in the N face n-GaN layer of the LED structure and via the bonding metal applying a compressive stress to the Si carrier substrate. The result of this curvature flip changes the bow of GLE from concave to convex relative to the p-GaN surface. This which has the effect of stretching the GLE adjacent to the Si carrier substrate causing the compressive stress in the emissive MQW to partially relax. By bonding the GLE to a 675 μm Si carrier substrate, a curvature flip of $\sim 3.4 \mu\text{m}$ was obtained. This curvature flip caused the MQW PL peak of a VLED to blue-shift to 448 nm from the MQW PL peak of 470 nm of the as-grown LED wafer. This corresponds to an increase of band gap energy of 130 meV. A larger curvature flip of $\sim 6 \mu\text{m}/\text{cm}$ was obtained by transferring the GLE to a thinner Si substrate of 475 μm as the thinner Si substrate is less rigid. An increase of band gap energy of 180 meV, which was further 50meV energy increase, was achieved. The light output power of the VLED bonded on to a 475 μm Si carrier substrate was 41mW at the drive current of 300mA, which was 8mW higher than the VLED bonded on to the 675 μm Si

carrier substrate. The VLED bonded on to a 475 μm Si carrier substrate showed an EQE of 23 % at 300 mA drive current, which was 4 % higher than that of VLED bonded on to a 675 μm Si carrier substrate. Although the two VLEDs having the same device structure, the one bonded to a thinner carrier substrate still showed a better EQE and stronger light output power due to the reduction in the QCSE effect. In addition, the I-V characteristic of the VLED bonded on the 475 μm Si carrier substrate only required 5.7 V to conduct 300 mA. While the one bonded on to 675 μm Si carrier substrate required 6.7 V to conduct 300 mA. These results suggest that transferring the GLE to a thinner substrate not only has a benefit of boosting the light output power and EQE, but also has a benefit of reducing the operational voltage.

6.6.References

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Chapter 7

Investigation of Surface Roughening For VLED

7.1. Introduction

The III-Nitride semiconductor material system has been widely used for optical communication, power electronic and video entertainment devices [1]. In particular, the recent successful commercialisation of Gallium Nitride (GaN) based blue emission light-emitting-diodes (LEDs) form the basis of solid state lighting. Despite this great commercial success, GaN based LEDs still suffer from several issues including poor light extraction efficiency (LEE) from the surface of the GaN LED epitaxy (GLE) to the air. This is because Snell's law states that a light ray will pass from a material of higher refractive index to one of lower refractive index only if its angle of incidence within the boundary between the two regions is less than a critical angle at which total internal reflection occurs. It is commonly known that the boundary of GaN and air has a low critical angle, calculated by Snell's law to be $\sim 23^\circ$, because GaN has a high refractive index of 2.5 [1] and air has a low refractive index of 1. As a consequence, light emitted by the LED active region which does not propagate within the small critical angle formed by the GaN and air boundary will not escape to the air and will remain within the GLE until it is scattered or more likely, re-absorbed [2]. This lowers the light extraction efficiency and thus reduces the external quantum efficiency (EQE). It is known that the critical angle can be improved by encapsulating the GaN surface. However, this increases the cost of device fabrication. Recently, Schnitzer et al. reported results of a ray tracing model that demonstrate roughening the top GaN surface of an LED can significantly increase the LEE [3]. Several research groups have successfully realized roughening or texturing of the surface of Ga polar GaN

grown on a sapphire substrate. For instance, Kim et al. enhanced the LEE by shaping the Ga polar GaN surface into a micro-lensed shape by using a photoresist re-flow and plasma etching method [4]. Hsieh et al. employed E-beam lithography to define a SiO₂ etch mask and precisely controlled the ICP plasma etching technique to transform a planar top surface of GaN into an array of pyramid shapes [5]. Although these two methods can increase LEE, they require additional complex processing steps. It is worth noting that, Na et al. [6], has successfully demonstrated that it is also viable to achieve surface roughening of the Ga face of the p-GaN layer of InGaN/GaN LED epitaxy grown on sapphire into an array of “pyramid cone” shape with diluted potassium hydroxide (KOH). The resultant surface features can significantly improve the LEE by introducing more chances for the light ray to escape from the LED [7]. However, since the next generation InGaN/GaN LED epitaxy will likely be grown on Si substrates for cost reasons, in order to improve the LEE of InGaN/GaN LED epitaxy grown on Si substrate, a vertical LED (VLED) structure must be adopted. This means that not only the top surface of the LED epitaxy needs to be roughened, but also requires the GLE removed from the original Si growth substrate and then bonded on to a foreign substrate with a reflective ohmic p-contact. Therefore, unlike the conventional lateral contact LEDs, where Ga face n-GaN is exposed, the N face n-GaN is instead exposed. It has been widely reported that the two basal planes of wurtzite GaN [0001] and [000 $\bar{1}$] can behave in significantly different manners. The Ga face basal plane [0001] is more chemically stable and has a smoother topology than the N face basal plane [000 $\bar{1}$] as described in Chapter 2.3. In addition, the KOH etch rate of N face GaN can be faster due to the etching mechanism of the KOH solution, in which the negatively charged OH ions react with the Ga atoms forming Ga₂O₃ and subsequently being dissolved by the KOH solution.

In this chapter, we investigate the surface topology of the N face n-GaN roughened in KOH and the effect of surface topology on the properties of the n-type contact. VLEDs with KOH treatment have also been fabricated, in order to investigate the actual impact of the KOH surface roughened N face n-GaN on the electrical and optical device performances.

7.2. Increase Light Extraction By Surface Roughening

Although GaN is an excellent wide band gap light emissive material, It is not a good material for the generated light to escape due to its high refractive index(n_{GaN}) of 2.5 [1] and air having a low refractive index(n_{air}) of 1. The boundary of GaN and air has a very low critical angle of $\sim 23^\circ$, calculated by using Snell's law. Therefore, light which does not travel within the critical angle will be confined within the LED as illustrated in Figure 7.1 and is likely being re-absorbed by the LED device material such as at the non-reflective metal contact or defects in the GaN epitaxy. This limits the LEE.

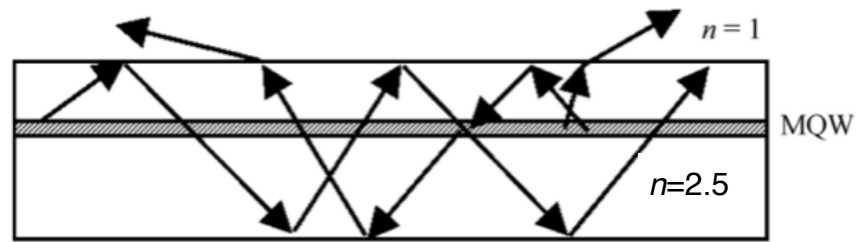


Figure 7.1: The light generated inside being confined within a semiconductor with high refractive index [8].

The most common method to improve the LEE is to use encapsulation. Since most of the encapsulant material has a refractive index of 1.5, the critical angle for the GaN to encapsulant interface is significantly increased. The encapsulant to air interface also has a large critical angle because of its smaller step in refractive index. Therefore, the LEE of a GaN based LED can be increased by using encapsulation. However, encapsulation can add extra cost to device fabrication. Recently, Lee et. al. proposed a ray tracing model demonstrating that roughening the top GaN surface of an LED can significantly increase the LEE [7]. Recently, Na et al. [6] have successfully demonstrated that surface texturing GaN grown on sapphire LED epitaxy of Ga polar into “pyramid cone” shape with diluted potassium hydroxide (KOH), which can significantly improve the LEE by introducing more chances for the light ray to escape from the LED [6] as illustrated in Figure 7.2.

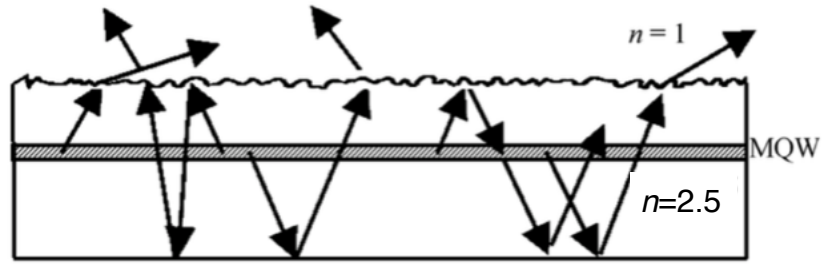


Figure 7.2: The light path in an LED with surface roughening [8].

7.3. Potassium Hydroxide (KOH) Texturing GaN Mechanism

GaN is well known for its chemical stability and cannot be etched in commonly used acids such as nitric, sulphuric and hydrochloric acids. Potassium Hydroxide (KOH), which is an inorganic compound, is one of the few known GaN etchants. However, aqueous KOH solution does not etch GaN uniformly and the etching is polarity (face) dependent. KOH etching of Ga face GaN is very slow and creates pyramid shaped pits where the threading dislocations emerge as illustrated in Figure 7.3(a) [9]. While KOH etching of N face GaN is fast and pyramid shaped cones with facets of $[10\bar{1}\bar{1}]$ plane are created as shown in Figure 7.3(b).

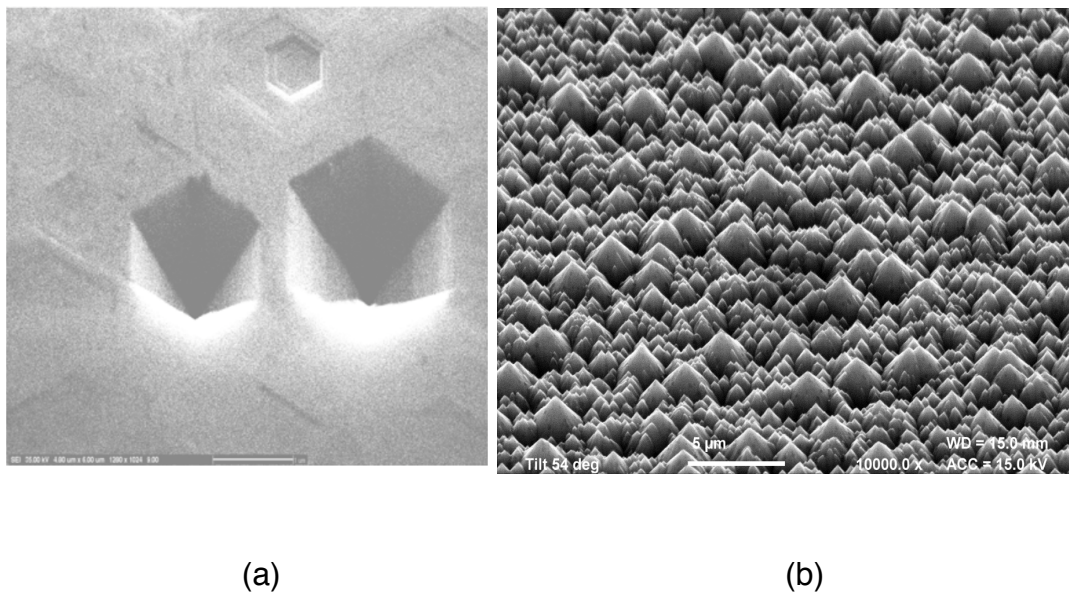
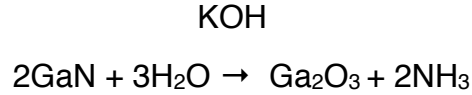


Figure 7.3: The SEM images of (a) Ga face GaN [9] and (b) N face GaN etching in aqueous KOH solution.

Aqueous KOH has two functions in etching the GaN; it first acts as a catalyst for oxidizing the GaN surface and secondly, it dissolves the oxidized Ga atoms. The oxidation reaction can be expressed as:



The difference in the etching behaviour between the two polarities can be attributed to the etching mechanism. As it can be seen in Figure 7.4, the negatively charged OH ions from the aqueous KOH solution first oxidize with the Ga atoms in the GaN surface to form Ga_2O_3 and the KOH subsequently dissolves these oxides [10]. However, the Ga face GaN has triple negatively charged occupied dangling bonds, which hinder the alike negatively charged OH ions from reacting with Ga atoms [10]. As a result, the KOH impact on Ga polar and N polar GaN during the KOH etch/roughening process can be significantly different.

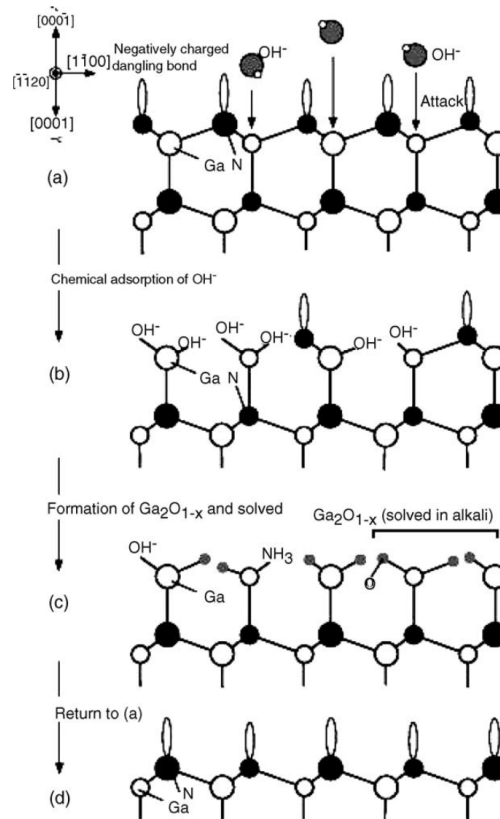


Figure 7.4: The schematics of (a) negatively charged hydroxide with N face GaN, (b) negatively charged hydroxide attacking Ga atoms, (c) formations of Ga_2O_3 on N face GaN surface, (d) the surface of N face GaN after dissolution of Ga_2O_3 [10].

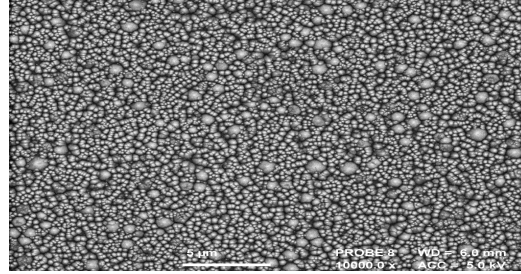
7.4. Experimental Details

In order to investigate the polarity dependence of KOH roughening, InGaN/GaN grown on Si LED wafer by metallorganic chemical vapour deposition (MOCVD), was supplied by Plessey Semiconductor Limited. This wafer has a 650 nm AlGaIn buffer layer with composition of 1470 nm n-GaN, 200nm thick InGaIn/GaN multiple quantum wells (MQWs) and 95 nm of p-GaN. Multi-layers of p-type ohmic contact of Ni/Ag/Ni (1 nm/200 nm/10 nm) were deposited on to the p-GaN of four LED samples by electron beam evaporation (EBE). These samples were then annealed in oxygen environment at 450 °C for 2 minutes, and samples were then wafer bonded on to a 475 μ m Si substrate with the procedures described in Chapter 3.8. The original Si substrates were then removed by the combination of mechanical lapping and SF₆ plasma. The unwanted AlGaIn layer was removed by Cl₂/Ar plasma to expose the N face n-GaN. KOH treatments of 2M, 3M and 4M were then applied to these samples. After the KOH treatments, the circular transmission line model (CTLM) structures suitable for n-type contact resistance testing and a n-type contact pattern were defined on the N face n-GaN using photolithography for subsequent lift-off. The n-type contact of Ti/Al/Ni/Au (20 nm/60 nm/20 nm/100 nm) were then deposited on to the N face n-GaN, again by EBE.

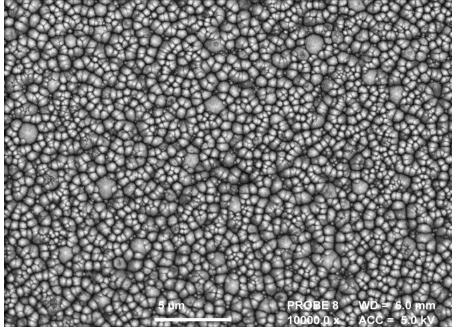
The surface topology of the sample was examined using a JOEL scanning electron microscope and the root mean square (RMS) surface roughness was obtained by using atomic force microscopy (AFM). To examine the n-type specific contact resistivity (ρ_c), current-voltage (I-V) characteristics of the CTLM test structure pattern were obtained by the method described in Chapter 3. The I-V characteristics of the VLED were measured using a Keithley 238 direct current source measurement. The light output of the Si-VLEDs was examined using an integrating sphere instrument with a Keithley 2600 pulsed source measure unit outputting 10ms duration current pulse.

7.5. Results and Discussions

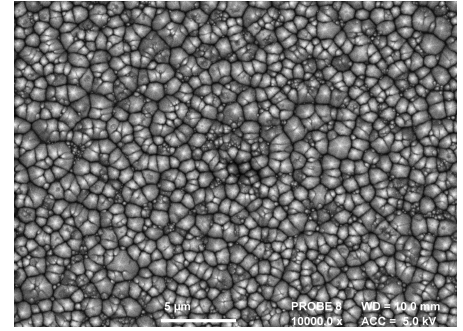
7.5.1. Surface Topology



(a)



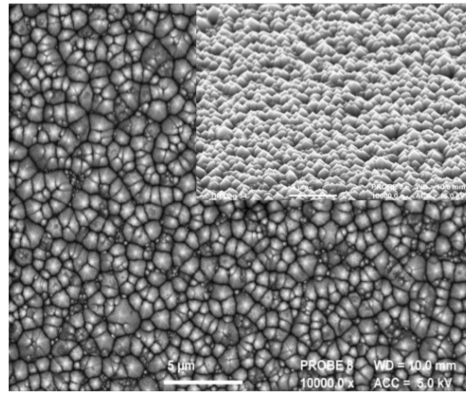
(b)



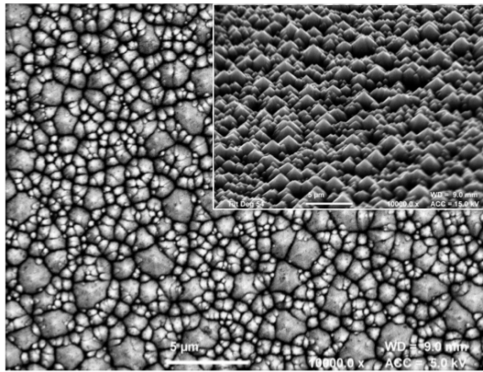
(c)

Figure 7.5: The SEM images obtained at 0° tilt of N face n-GaN roughened using 2M KOH for (a) 1 minute, (b) 2 minutes and (c) 3 minutes at 100 °C.

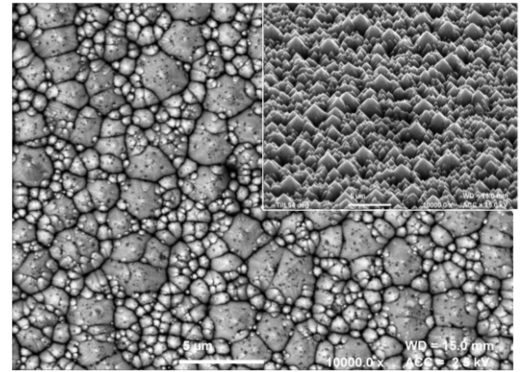
Figure 7.5 shows scanning electron microscopy images (SEM) of surface morphology obtained at 0° tilt of N face n-GaN roughened using 2M concentration of KOH solution at 100 °C for (a) 1 minute, (b) 2 minutes and (c) 3 minutes. It can be seen that all three samples appear to have a hexagonal cone-like pyramid morphology after etching in KOH solution and the average feature size of the cone like pyramids increased as the duration of the etching process increased. The root mean square (RMS) roughness of the surface was increased from ~ 57 nm for 1 minute 2M KOH treatment, to ~ 81 nm after etching in the 2M KOH solution for 3 minutes.



(a)



(b)



(c)

Figure 7.6: SEM images taken at 0° tilt and 54° tilt (inset) of the surface topologies of N face n-GaN after (a) 2M KOH, (b) 3M KOH and (c) 4M KOH for 3 minutes.

Figure 7.6 shows SEM images of the N face n-GaN surface dipped into (a) 2M, (b) 3M and (c) 4M KOH solutions with various concentration for 3 minutes etching time. The 0° tilt images reveal generally high density but disordered nature of these pyramids. The insets were obtained at 54° tilt, compared with 0° tilt for the main images. It can be seen from the insets that in each case the N face n-GaN surface is covered in dense disordered arrays of “cone-like” pyramids. Varying the KOH solution concentration from 2M to 4M has a similar systematic effect as increasing the etch time on the “cone-like” pyramid feature size. As the concentration of the KOH solution increased, the pyramid feature size increased and also the pyramid features became significantly sharper. The RMS roughness increased from 81 nm for 2M to 181 nm for 4M KOH treatment, both with 3 minute etch duration. This can be attributed to a sufficient availability of OH ions to give continuous rapid GaN etching. Increasing the KOH concentration leads to more OH ions being available to react with the Ga atoms,

which makes etching process more aggressive, resulting in a faster pyramid formation.

7.5.2. Electrical and Optical Properties

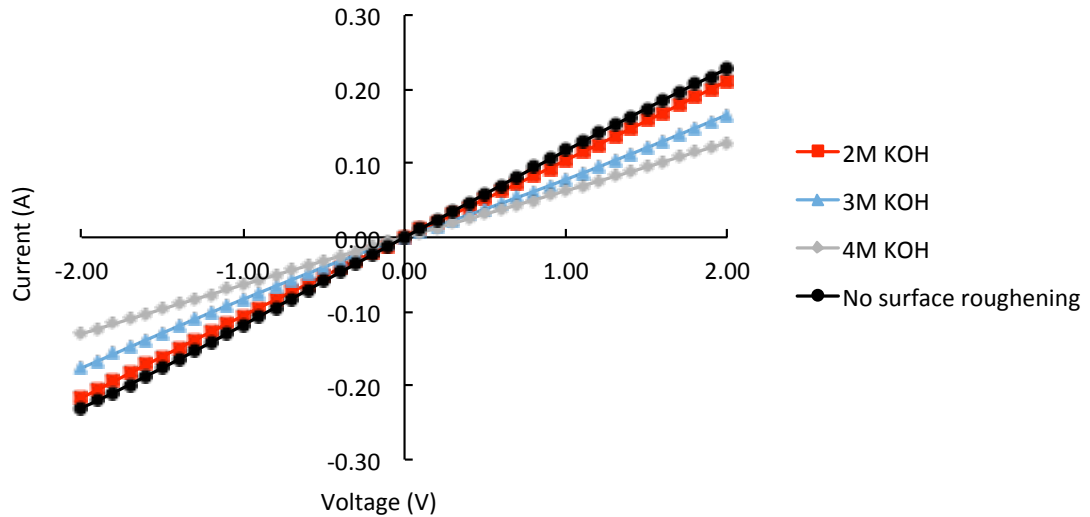


Figure 7.7: The I-V characteristics of Ti/Al/Ni/Au (20 nm/60 nm/20 nm/200 nm) contact deposited on as grown and KOH treated N face n-GaN surfaces.

Since the surface morphology of N face n-GaN can vary significantly under different concentration of KOH solution, It is very important to understand the impact of this surface morphology on the n-type contact. Figure 7.7 presents the I-V characteristics of the two CTLM test structures for the standard n-type ohmic contact of Ti/Al/Ni/Au (20 nm/60 nm/20 nm/200 nm) deposited on N face n-GaN surfaces roughened in 2M, 3M and 4M KOH solution for 3 minutes at 100 °C. The I-V characteristic of the CTLM test structure formed on the as grown, N face n-GaN surface is shown for comparison. It was found that the roughened and smooth GaN surfaces do not have a direct impact of the ohmic contact behaviour. However, the contact became less conducting as the KOH concentration increased. It was initially conducting 2.28×10^{-1} A at 2 V for contact deposited on an unroughened n-GaN surface and only conducting 2.11×10^{-1} A at 2 V after etching in 2M KOH solution, equivalent to ~8 % reduction in effective sheet conductivity. When the the concentration of KOH solution increased to 4M, the contact could only conduct 1.28×10^{-1} A current at 2 V applied biased, equivalent to a ~ 44 % reduction in effective sheet conductivity.

| KOH Concentration | Contact Resistivity (Ωcm^2) |
|----------------------|---|
| No surface treatment | 1.22×10^{-4} |
| 2M | 1.58×10^{-4} |
| 3M | 4.94×10^{-4} |
| 4M | 6.59×10^{-4} |

Table 7.1: Contact resistivity of Ti/Al/Ni/Au (20 nm/60 nm/20 nm/100 nm) contact deposited on N face n-GaN with KOH surface roughening.

Table 5 shows the specific contact resistivity of the Ti/Al/Ni/Au contact deposited on N face n-GaN etched in 2M, 3M, 4M KOH solution for 3 minutes at 100°C and the bare N face n-GaN surface without KOH treatment. The surface without KOH treatment provided the best contact resistivity of $1.22 \times 10^{-4} \Omega\text{cm}^2$. The specific contact resistivity of the KOH treated surface increased as the KOH concentration became stronger. It was measured to be the highest, $6.59 \times 10^{-4} \Omega\text{cm}^2$, for the sample etched in 4M and the lowest, $1.58 \times 10^{-4} \Omega\text{cm}^2$, for the sample etched in 2M. This can be attributed to the poor metal contact coverage of the “cone-like” pyramids caused by the KOH etching of the N face n-GaN surface. As illustrated in Figure 7.8 that the n-contact deposited on VLED with and without the KOH treated N face n-GaN surface. In addition, metal layer deposited on a roughened surface will have a tendency for cracks to occur in the metal films at the top and bottom of sharp-edged features. The VLED without the KOH treatment can provide a good contact resistivity because the much smoother surface enables a good metal contact coverage. However, such a surface does not provide a good LEE due to the small critical angle of $\sim 23^\circ$. Figure 7.8(b) illustrates the light output VLED with the KOH roughened surface, which can increase the LEE by introducing light scattering centres. However, it can simultaneously induce a poor contact resistivity to n-GaN due to poor metal step coverage.

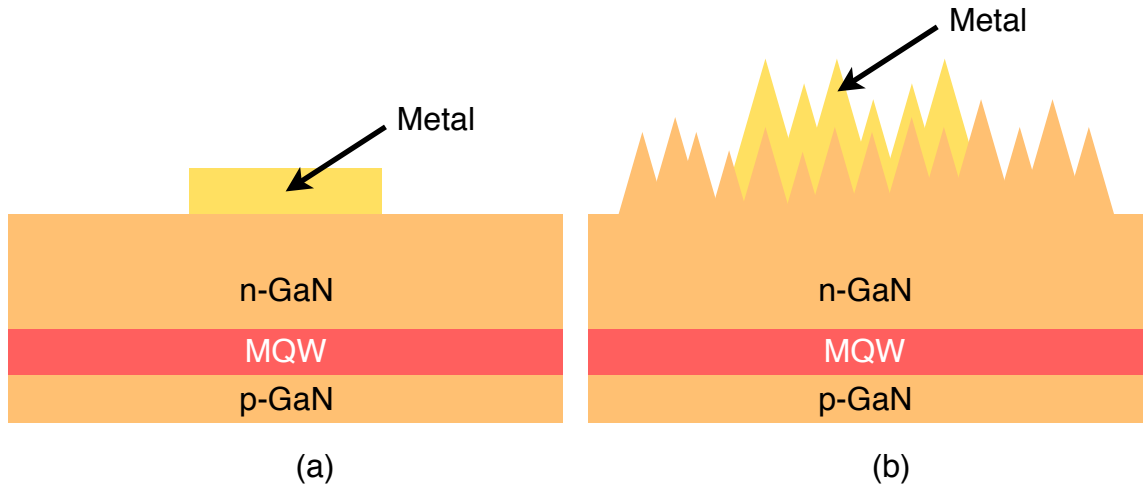


Figure 7.8: The schematics of of VLED (a) without and (b) with KOH surface roughening treatment.

Figure 7.9 illustrates the light output power of 1 mm² VLED devices without surface roughening and with 2M KOH surface roughening treatments of 2 and 3 minutes at 100 °C as a function of drive current. Both VLEDs with a KOH treatment showed a higher light output than that of the VLED with a smooth n-GaN surface. The normal VLED only showed a 53 mW light output power at 300 mA. However, when the VLED was treated with 2M KOH solution for 2 and 3 minutes at 100 °C, the light output power increased to 58 mW and 62 mW respectively. This can be attributed to the increase in RMS roughness of the N face n-GaN surface.

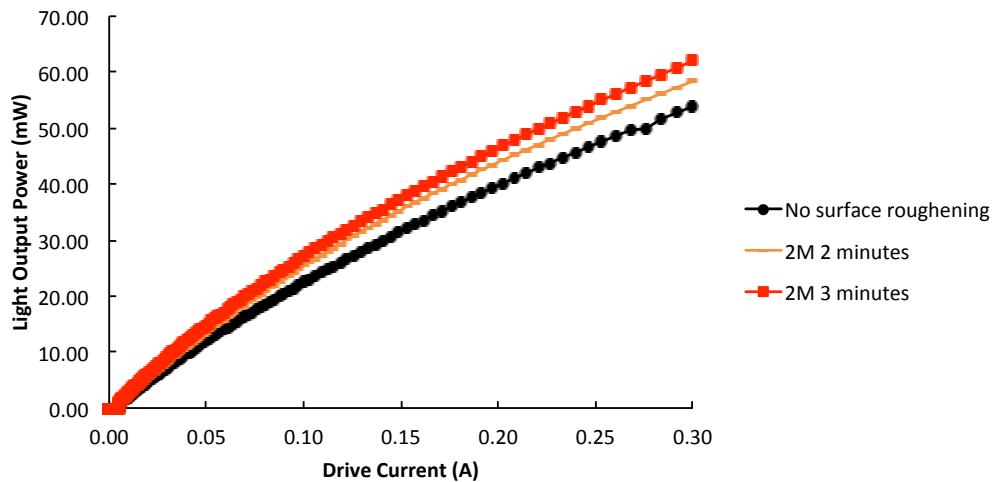


Figure 7.9: The light output power of VLEDs with no surface roughening and with 2M KOH for 2 and 3 minutes at 100 °C as a function of drive current.

Figure 7.10 illustrates the the I-V characteristics of 1 mm² VLED devices without surface roughening and with 2M KOH surface roughening treatment for 2 and 3

minutes at 100 °C. The VLED devices after the KOH treatment showed degraded electrical behaviour. The device with an unroughened surface only required an operational voltage of 4.93 V pass a drive current of 300 mA. However, as the pyramidal surface became more pronounced after the KOH surface roughening process, the contact resistivity increased. Specifically, operational voltage of the 2M KOH roughening for 2 and 3 minutes immediately increased to 5.85 V and 6.2 V respectively.

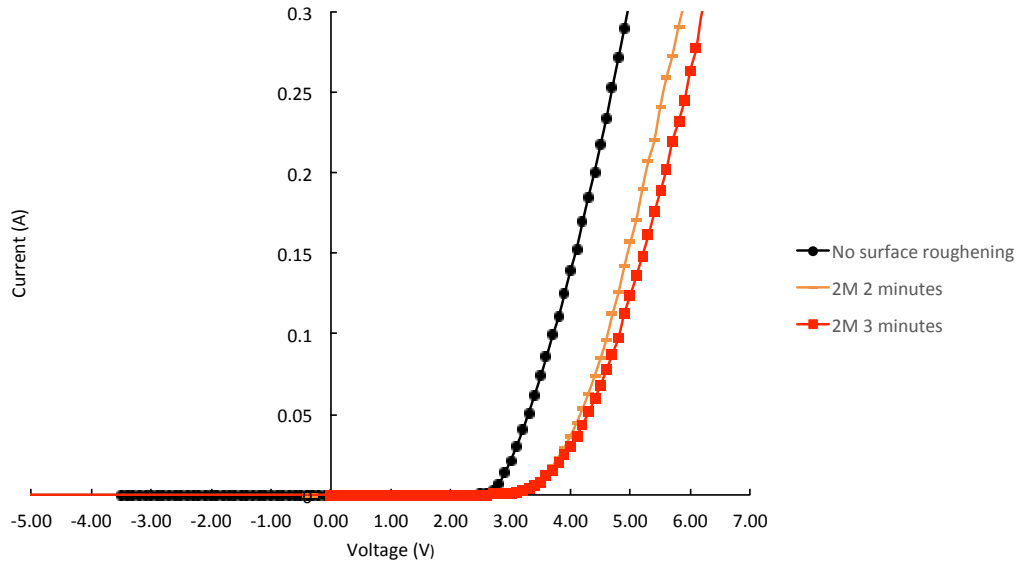


Figure 7.10: The I-V characterisations of normal VLEDs and VLEDs with the n-GaN surface roughened in 2M KOH for 2 and 3 minutes.

In order to investigate the impact of various KOH concentrations on the device electrical performance, the I-V characteristics of VLEDs with and without KOH treatment were measured. Figure 7.11 illustrates the I-V characteristics of 1 mm² VLED devices with and without KOH surface roughening treatment for 3 minutes at 100 °C as a function of drive voltage. The operational voltage of the VLED device without KOH treatment was clearly the lowest compared to those measured from the KOH treated VLEDs. It only required an operational voltage of 4.93 V to inject a current of 300mA. In contrast, the VLED etched in 3M and 4M KOH solution with rough morphology required an operational voltage of 7.5 V and 8.3 V under the same current injection level, respectively. It is worth noting that as the concentration of KOH solution increased, the operational voltage of the VLED also increased. This can be attributed to the roughness induced poor contact resistivity.

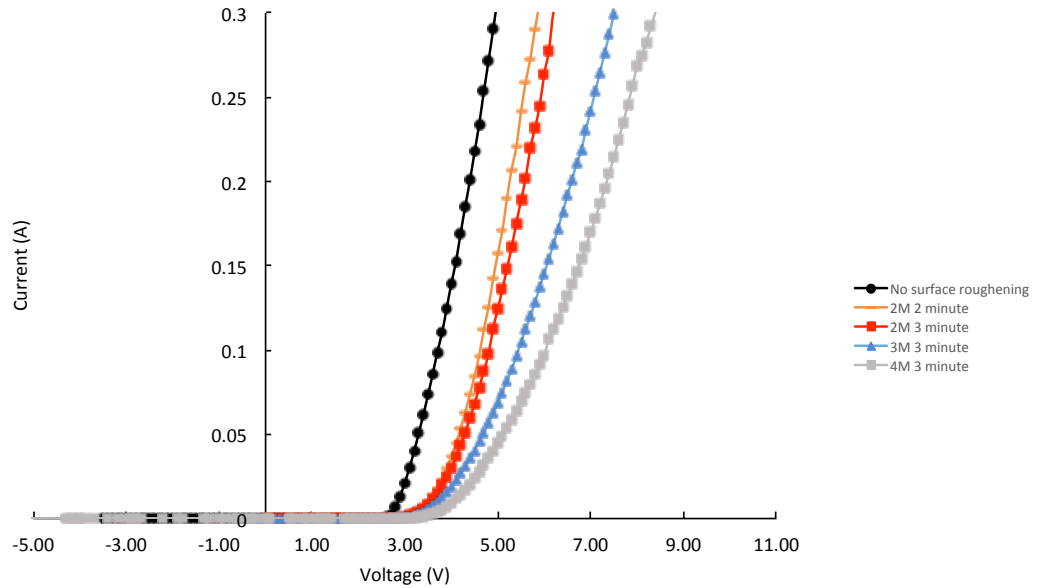


Figure 7.11: The I-V characteristics of VLED devices without any surface treatment and with 2M, 3M and 4M KOH treatment for 3 minutes at 100 °C.

Since the surface morphology appears to have a great impact on the I-V characteristics of the VLED, it is very important to understand the impact of roughened surface on the device wall plug efficiency. Figure 7.12 illustrates the light output power measured from a conventional VLED and VLED with KOH treatments under various concentration as a function of drive current. The VLED etched in 2M, 3M and 4M KOH solutions showed 62 mW, 76 mW and 97 mW of light output powers under 300 mA of drive current, respectively. It is evident that as the concentration of KOH solution increased, the light output power of the KOH treated VLED also increased. This suggests that increasing the RMS surface roughness improves the light extraction. Specifically, the VLED went through the 4M KOH roughening process produced the strongest light output amongst all VLED samples. Its light output power is nearly 1.8 factor higher that the conventional VLED without any surface treatment.

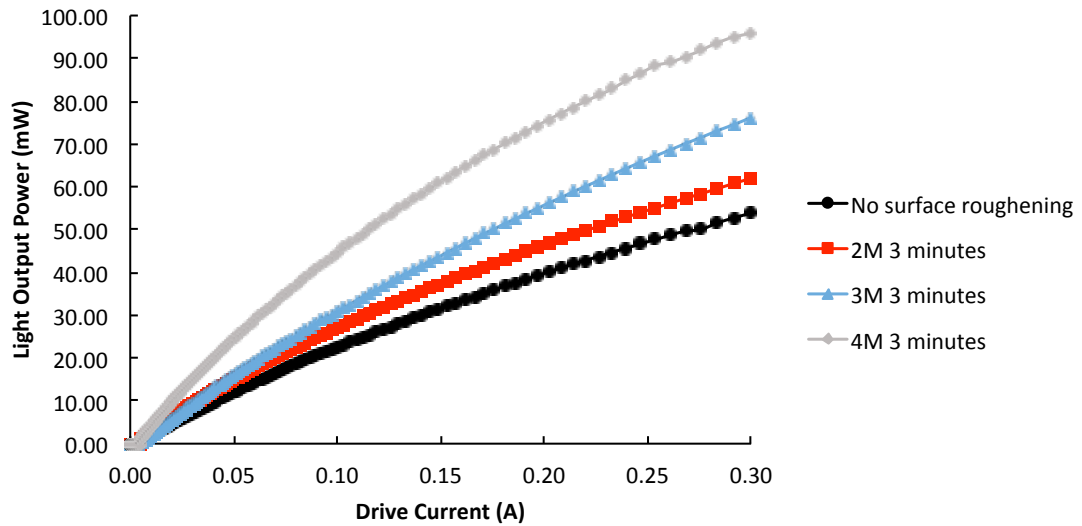


Figure 7.12: The light output power of VLEDs with 2M, 3M, 4M KOH treatments for 3 minutes and without KOH treatments.

In order to evaluate the impact of surface morphology on the overall device performance, the wall-plug efficiencies (WPEs) of the VLEDs treated with various concentration of KOH solution are compared with that of a VLED with an unroughened surface as a function of drive current in Figure 7.13. The VLED roughened in 4M KOH solution showed a WPE of 72 mW/W at 100 mA of drive current, which is the highest amongst all VLED samples considered here. This result indicates that VLED treated in 4M KOH solution was the most efficient converting the electrical power into light output power, despite the surface roughening process causing the greatest degradation of the I-V characteristics via the etch-induced increase in contact resistance. However, there is no clear trend in WPE with KOH etch concentration. Although the 3M KOH VLED sample showed a higher light output power than the conventional VLED sample and 2M KOH VLED sample, its WPE at 100 mA is 51 mW/W, which is 10 mW/W and 3 mW/W lower than those of conventional VLED and 2M KOH VLED samples. This can be attributed to the increase in LEE being insufficient to counteract the degradation of the I-V characteristics. The 3M KOH VLED only enhanced the light output power by 43 % factor of the conventional VLED. However, it required a 50.1 % higher forward voltage than the conventional VLED to achieve this.

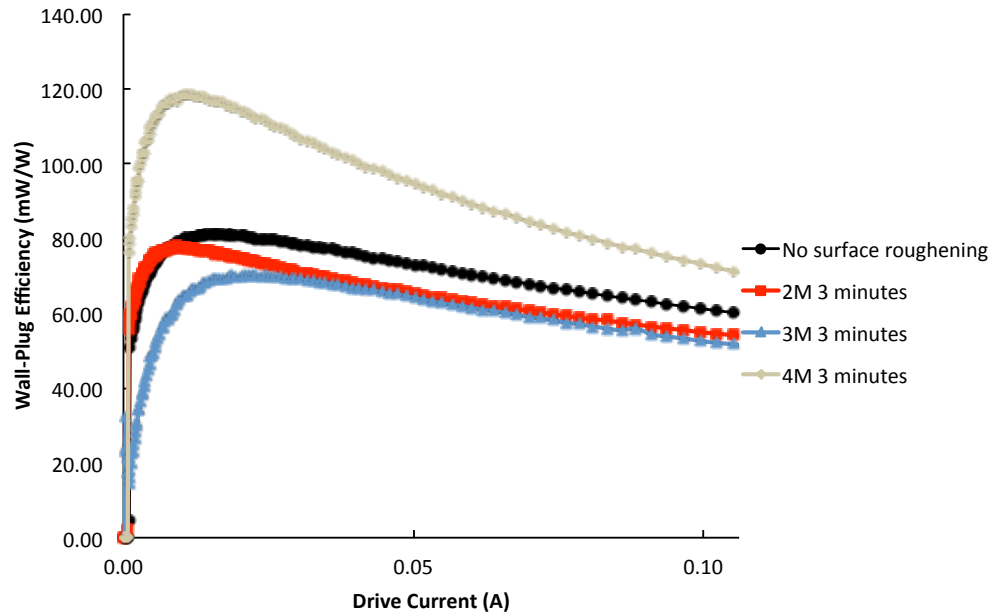


Figure 7.13: The Wall-Plug efficiency of VLEDs with 2M, 3M, 4M KOH treatments for 3 minutes and without KOH treatments.

7.6. Conclusion

GaN on Si VLEDs with Ni/Ag/Ni contact developed in Chapter 3 were fabricated for the investigation of KOH surface roughening impact on the electrical and optical properties of the VLEDs. It was found that the KOH surface roughening had a great impact on the electrical and optical properties of the VLED. The low critical angle issue with the GaN and air interface was resolved by roughening the surface with KOH solution. However, roughening the surface also degrades on the electrical characteristics of the LEDs. The bare N face n-GaN surface provided the best n-type contact resistivity of $1.22 \times 10^{-4} \Omega \text{cm}^2$. However, when the n-GaN surface was etched in the KOH solution, the contact resistivity increased from $1.52 \times 10^{-4} \Omega \text{cm}^2$ to $6.59 \times 10^{-4} \Omega \text{cm}^2$ for 2M KOH to 4M KOH solution. A likely cause of this is the lumpy surface induced poor metal contact step coverage. According to the device I-V characteristics measured from the conventional VLED and VLED etched in various various concentration of the KOH solution, it was found that VLED etched in 4M KOH solution required the highest operational voltage of 8.4 V to conduct 300 mA of current. Under the same drive current level, It only required nearly 4.93 V and 6.2 V for the conventional VLEDs and VLEDs etched in 2M KOH solution. The degraded electrical behaviour can be attributed to an increase in the effective sheet

resistivity of the contact metals caused by poor step coverage of the cone-like pyramid features. It was determined that as the n-GaN surface RMS roughness increased, the light output power also increased. This result indicates that increasing the size of the pyramid features on the n-GaN surface can also increase the light output power. By etching the VLED in a 4M KOH solution at 100 °C for 3 minutes can boost the light output power by 83 % compared to the conventional VLED. According to the results of WPEs of all the VLEDs, it was found that 4M KOH VLED showed the highest WPE compared to the conventional VLED and VLED treated in 2M and 3M KOH solutions. Although the 3M KOH VLED had the second highest light output power, it had the worst efficiency on converting electrical power to light output power. This can be attributed to the small light output enhancement compared to the increase in the additional forward voltage. Finally, the poor step coverage can be compensated in two ways: Sputtering can be used to deposit n-contact metal layers, or these can be deposit prior to roughening the N face n-GaN through which light is emitted. The latter method would involve an extra photolithography step, but a low n-type contact resistivity can potentially be obtained.

7.7.References

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Chapter 8

Summary and Outlook

8.1.Summary

Although Light Emitting Diodes (LEDs) are the most efficient light source. However, it was not used as a domestic lighting source until Gallium Nitrides (GaN) based LED was invented in 1992. This is because a blue LED is vital to generate white light with both the phosphor coating and combining the three primary colour methods. Before 1992, there was no suitable direct wide band gap material to fabricate blue LEDs. The invention of GaN based blue LEDs re-attracted the attention of researchers and manufacturers for using LEDs as the domestic light source due to its excellent optoelectronic property. The GaN based LED epitaxy is conventionally grown on a sapphire substrate. However, Sapphire is expensive, thermally and electrically insulating. As a consequence, the researchers and manufacturers have started their interest of growing GaN based LED epitaxy on a Silicon (Si) substrate as it is electrically conducting and available at large size with a much lower cost. However, Si substrate is not transparent and absorbs the light emitted by the multiple quantum wells (MQWs), resulting in lower light extraction efficiency (LEE). As a consequence, this work has developed a vertical LED structure with wafer bonding technique fabrication process for the GaN based LED epitaxy grown on Si substrate to resolve the LEE issue: the original Si growth substrate is removed and the GaN based LED epitaxy is bonded on to another Si carrier substrate with an reflective ohmic contact in between. Developing a good ohmic contact to p-GaN is challenging, in particular for the p-type contact for p-GaN on Si VLED structure as it is difficult to find metals with work functions larger than that of p-GaN ($\Phi_{p\text{-GaN}} = 6.5 \text{ eV}$). In addition, the p-type contact for VLED structure not only to provide a low contact resistivity to p-GaN, but also needs to be highly reflective to reflect to the light that propagates towards the Si carrier substrate.

In Chapter 4, We successfully developed an p-type ohmic contact for our VLED by using Ni/Ag/Ni (1 nm/200 nm/10 nm). It had a very contact resistivity of $6.3 \times 10^{-5} \Omega \text{cm}^2$ and a high contact reflectivity of 75 % after annealing in oxygen for 2 minutes to form ohmic contact to p-GaN. During the development, different combination of Ag based contacts was systematically studied. It was found that the Ag only contact became an ohmic contact after annealing in an oxygen environment at 350 °C for 2 minutes. The ohmic contact behaviour was attributed to the increase in the hole concentration near the p-GaN surface due to Ga atoms out-diffusion into the Ag contact. However, the Ag only contact was not thermally stable, it experienced a contact resistivity and reflectivity degradation for annealing temperature above 350 °C due to Ag agglomeration. By inserting a thin layer of Ni, the Ag agglomeration was found to be less significantly mitigated and the Ni/Ag was found to be more thermally stable. The contact reflectivity and reflectivity were found to be improved. We also found that the Ag agglomeration can be prevented by capping the Ni/Ag contact with 10 nm of Ni layer. The resultant Ni/Ag/Ni contact only had a 12 % of reflectivity degradation and showed a contact resistivity in the order of $\sim 10^{-5} \Omega \text{cm}^2$ after annealing in oxygen for 2 minutes.

In Chapter 5, the impact of Si carrier substrate thickness on the LED device performance was investigated. It was found that the unprocessed bare LED wafer has a pre-existing concave curvature of $\sim 1.2 \mu\text{m}$ due to the tensile stress. However, when the GaN based LED epitaxy (GLE) was bonded on to the carrier substrate with a thickness of $675 \mu\text{m}$, the curvature was reversed to a convex curvature of $4 \mu\text{m}$. From the result of dynamic photoluminescence (DPL) of the GaN layers on the unprocessed LED wafer, it was determined that the GaN PL peak blue shifted from $\sim 366.8 \text{ nm}$ to $\sim 364.2 \text{ nm}$, as the laser beam moved from the top of the GLE towards the Si growth substrate. This result revealed that the top part of the GLE has a larger tensile stress than the bottom part of the GLE. However, the DPL of the GaN layers on the VLED bonded on to the Si carrier with $675 \mu\text{m}$ showed a larger range of GaN peak variation (i.e. from $\sim 362.8 \text{ nm}$ to $\sim 367.8 \text{ nm}$) and the GaN PL peak experienced a red shift as opposed to the blue shift on the unprocessed LED wafer. This suggests the top part of the GLE has a lower tensile compared to the bottom GLE. The relaxation of the tensile

stress on the top part of the GLE can be attributed to the removal of the original Si growth substrate, causing the top GLE to shrink back to its original room temperature size. While the reversal of the curvature has an effect of stretching the bottom part of the GLE to apply the tensile stress, resulting in the red shift of the GaN peak. It was identified that the MQW PL peak of the GLE bonded on to a 675 μm Si carrier substrate blue shifted to 448 nm from 470 nm. This can be attributed to the reversal of curvature, which applied a further tensile to the bottom part of the GLE to reduce the compressive stress inside the MQW and the quantum-confined stark effect (QCSE). It was also noticed that when the GLE was bonded on to a thinner Si carrier substrate of 475 μm , the curvature increased from $\sim 4 \mu\text{m}$ to $\sim 6 \mu\text{m}$. This is because a thinner Si substrate is more flexible. The MQW PL peak of the GLE bonded on to a 475 μm was found to blue-shift to 441 nm. This can be explained by the further reduction of QCSE by the increase in the curvature of the thinner Si carrier substrate, resulting in a larger tensile stress applied to the bottom part of the GLE. It is worth noting that using a thinner Si carrier substrate not only reduced QCSE, but also reduced the operational voltage as the voltage drop across the thinner substrate was smaller than that of the thicker substrate.

In Chapter 6, GaN based VLEDs with optimized reflective p-type ohmic contact of Ni/Ag/Ni and curvature were fabricated for the investigation of KOH surface treatment to resolve the low critical angle between the interface of GaN and air. We successfully developed a KOH roughening process for our VLED, which increased the light output power from 53 mW to 97 mW. During the development, It was found that the N face n-GaN surface became hexagonal “cone-like” pyramids after etching in KOH solution and the pyramid size increased with the etching time and the concentration of KOH solution. Roughening the top surface of a VLED had a great impact on the light output power. The VLED without any surface treatment only outputted 53 mW of light output power. By etching the VLED into 3M and 4M KOH solutions at 100 °C for 3 minutes, the light output power was boosted to 76 mW and 97 mW. However, the pyramid features on the n-GaN also had an impact on the electrical performance. The forward voltage of the VLED increased from 4.93 V to 7.5 V and 8.3 V to conduct 300 mA of current after etching in 3M and 4M KOH

solutions, respectively. It was found that the VLED etched into 4M KOH solution had the best efficiency of converting electrical power to light output power.

8.2.Outlook

The GaN/InGaN LED epitaxy grown on Si (111) technology has been widely adopted by the domestic light application industries due to low cost of Si substrates. Because of the light absorbing nature of Si growth, the vertical LED structure must be adopted to maximize the light output power for the GaN LED epitaxy grown on a Si substrate. The fabrication process of the VLED tends to be very lengthy, complicated and expensive. This is because it involves depositing several thick layers of wafer bonding metals, the cost of high conductivity of Si carrier substrates and also removing the original Si growth substrate. As a consequence, it is very important to minimize the fabrication steps and cost for the industrial point of view. Although the fabrication process in this work is low cost as it does not involve gold in the wafer bonding process, it is still relatively expensive to implement compared to the conventional lateral contact LED. An improvement can be made in the existing fabrication process to minimize the cost. In stead of bonding the LED wafer to a high conductivity Si carrier substrate, a copper (Cu) substrate with a thickness of $\sim 200\ \mu\text{m}$ to $\sim 300\ \mu\text{m}$ can be electroplated to the LED wafer as the mechanical support. This can effectively lower the cost of fabrication as It only requires 100 nm-200 nm of Cu as the seed layer and electroplating 100 to 200 μm of Cu. The relatively high cost of thick bonding metals and high conductivity Si carrier substrate are no longer required. In addition, although the p-type and n-type contacts of the VLEDs fabricated in this work are optimised, the turn-on voltage is believed not optimized as there is an additional voltage dropped across the Si carrier substrate. To reduce this additional voltage, the thickness of the Si carrier substrate can be reduced. However, this will add an extra step to the existing fabrication process. By using electroplated Cu as the carrier substrate, the post Si carrier substrate lapping process is not required as the voltage drop across Cu is very low due to electrical resistivity of Cu (i.e.16.78 n Ωm at 20 °C). Thus, using Cu electroplating technique as the carrier substrate in stead of Si substrate not only can improve the device performance, but also can effectively reduce the fabrication cost.

In addition, as it can be seen in Chapter 5 that although the surface roughening the VLED can significantly improve the light output power. However, it inevitably comes with a forward voltage degradation, which can decrease the wall-plug efficiency. An improvement can be made during the surface roughening step. A SiO_2 etch mask can be deposited to protect the n-GaN area for n-type electrode from the KOH etch. This means that the non-metal contact area will only be roughened and leave the area for the n-type electrode intact. This can preserve the contact resistivity while improving the light output power.